

AXIe Local Bus Architecture Delivers Unprecedented Bus Speeds

By [Larry Desjardin, Modular Methods](#) and [Lauri Viitas, Guzik Test and Measurement](#)

AXIe is commonly referred to as the “big brother” of PXI. This is because it shares many of the features of PXI (open modular structure, PCI Express fabric, similar software) while deploying a large board size, power, and cooling matching that found in high performance instruments. However, it also adds one very unique aspect: the AXIe local bus. In this paper the authors describe the local bus, its capabilities, and recently announced products that demonstrate breakthrough system performance utilizing the local bus. These capabilities include real time streaming and processing in excess of 40GB/s per link.

Real time high-speed streaming enables a number of applications previously unrealized. Radar system evaluation and simulation is an example, where data is streamed indefinitely from high-speed digitizers into a data processing module or RAID array. High-energy physics is another example where data is recorded for long periods, to be triggered by an event that is detected by a digital processor unit. Indeed, there is a broad range of data acquisition applications where long data streams need to be recorded or processed while searching for an intermittent event. The AXIe local bus enables this capability at previously unattainable speeds.

Bus Topologies: A Little Background

A modular backplane, such as VXI, PXI, or AXIe, consists of a PCB (printed circuit board) with copper paths creating buses between the various slots. In this sense a modular backplane is not a single bus, but several buses, each bringing unique functionality. The geometric pattern of each bus is called its topology. There are three common bus topologies in a modular standard: [parallel](#), [star](#) and [local](#).

Three Bus Topologies: Star, Parallel, and Local

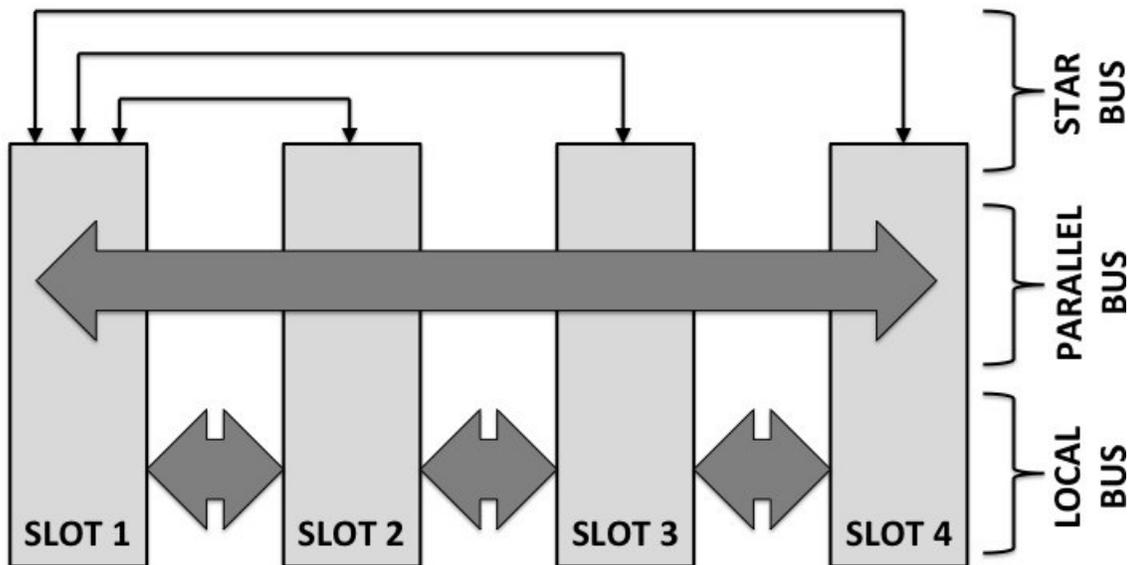


Figure 1. The diagram shows three bus topologies common in computer and instrumentation systems. Slot 1 acts as the hub for the star bus. The parallel bus spans all slots. The local bus is segmented, connecting only between adjacent slots.

These topologies are critical to modular instruments and are the basics that enable many of the unique features that modular instrumentation brings to the marketplace. A quick review of each is given below:

Parallel (also called multidrop). Until recently, this was the most common bus topology: a structure where the same pin on each slot is electrically connected to the similar pin on all other slots. Instrument and computer data buses used this topology ubiquitously through the early 2000s, before the advent of serial buses. VXI and PXI-1 (pre PXI Express) use a parallel bus for data transfer. In a parallel bus the data is present across all slots, and the address determines which slot is being written to.

Parallel buses are also used for many trigger and clock lines. Here, a signal from one device can trigger one or more other devices, since all devices have access to these parallel lines. Clock signals can be routed in this manner as well. VXI, PXI, and AXIe all have some number of parallel trigger lines. The parallel topology is a very useful topology, but suffers one key defect: speed. The large number of loads plus the stubs created at each slot limit the top bus speeds to the neighborhood of 100MHz. Even if 100MHz can be achieved, the slow edge ramps make parallel buses largely unsuitable for precision timing. This was a fundamental limit for computer backplanes, which led the industry to embrace serial designs that use a star topology.

Star. In a star topology, one device is a “hub” and has a separate dedicated line going to each slot. Visually, these are like rays coming from a star, thus the name “star”. These are typically differential pairs, called lanes. Since each lane is point-to-point, it can be operated at much higher speeds. When the clock is encoded within the data pattern itself, it is referred to as a serial bus. Very high speeds are possible with point-to-point serial buses. Gen 1 (Generation 1) of

PCIe (PCI Express, the data bus for VXI 4.0, PXI Express, and AXIe) enables 2.5Gb/s (2.5 Gigabit per second) on each lane. Using a common 4-lane link (a link is a bundle of lanes), PCIe can transfer data at 1GB/s (One Gigabyte per second, where each byte is 8 bits). Due to the high speeds to be discussed, this paper will use units of GB/s going forward.

PCIe Gen 2 essentially doubles the speed of the first generation PCIe. Many PXIe and AXIe products now deploy PCIe Gen2, doubling the speed of a 4-lane link to 2GB/s. PXIe chassis support 8-lane links, doubling the speed again. While these speeds are impressive, and much higher than USB or LAN interfaces found on traditional instruments, they do not match the speed of ultra-fast data converters. This is where the third topology, the local bus, makes a disruptive contribution.

Local bus. Also called a segmented bus or daisy chain bus. This is a unique bus structure that brings a lot of hidden benefits. Local buses are a set of short copper segments that connect pins between adjacent slots. This is why they are called “local” buses. For example, the right side of slot 2 is connected to the left side of slot 3. Then the right side of slot 3 is connected to the left side of slot 4, and so forth. Because the copper path lengths are short, only a few centimeters, very high-speed signals can be routed from slot to slot. Local buses enable high-speed private communication between related modules of an instrument set. Since the local bus begins and ends between the modules of an instrument set, another set of modules may use their local buses completely differently. This way, instrument sets from different vendors may co-exist in the same chassis, each exploiting the unique capabilities of the local bus.

Local buses are not new to modular instrumentation. VXI deployed a 12-line local bus (12 copper paths between each adjacent slot). The [Agilent 81250 ParBERT](#) is a good example of how it was used to extend private timing signals to all modules to create a modular bit error rate tester. PXI adopted a 13-line local bus, and some digital products exploited this. Unfortunately, these pins conflicted with pins defined in the PXIe (PXI Express) standard, leaving only a single remaining local bus line. For this reason, the local bus is rarely, if ever, used in PXIe systems.

AXIe reintroduced the local bus concept, but at the scale to match its high performance mission. The AXIe local bus consists of 124 lines organized as 62 high-speed differential pairs. With 60 pairs dedicated to a data path, and using fairly common FPGA (field programmable gate array) SERDES (Serializer/Deserializer) technology, the aggregate bus bandwidth totals 40GB/s from one slot to the next. This is an order of magnitude beyond other bus structures. Since AXIe only defines the topology of the local bus, the aggregate bandwidth will increase proportionally with the interface bus speeds deployed. Newly announced FPGA SERDES speeds should double the aggregate bandwidth to 80GB/s, with the next wave doubling it again to 160GB/s. Since this is the speed of each segment between slots, and each segment acts independently, a large AXIe system can support aggregate chassis bandwidths into the TB/s (Terabyte/sec) range. Now, that is some bandwidth!

Real Products and Applications

The sections above give a theoretical description of the local bus. The [Guzik family of digitizers](#) takes advantage of the local bus bandwidths. Announced previously, the Guzik ADC6000 series is essentially a family of high-fidelity 8-bit digitizers based on an aggregate 40Gs/s sampling rate. Single-slot AXIe products include the following digitizing combinations:

- 1 channel x 40Gs/s
- 2 channel x 20Gs/s

4 channel x 10Gs/s

Each product hosts 64GB of memory, allowing a single shot waveform capture of greater than one second at full speed. Since the aggregate data generation of each digitizer is 40GB/s, the local bus interface can support full speed data transfer to the adjacent slot. The digitizers accept data from the left, and source it to the right. This allows digitizers to be chained together, useful for sharing memory between digitizers in order to expand the single shot capture window proportionally. While proving that AXIe can support 40GB/s rates over the local bus, without additional modules this had limited utility. It is the recent introduction of a digital processing module that demonstrates the powerful capabilities enabled by the AXIe local bus.

Enter Digital Processing

Guzik is now introducing the AXIe DP 6000 Digital Processor Module, which is local bus enabled. The DP 6000 hosts two large user-configurable Altera Stratix V FPGAs, each delivering 3,550 multipliers and 583,000 logic elements, and has 64GB of on-board memory. This product highlights a number of the advantages of the AXIe local bus architecture. Like the digitizers, it accepts data from the left, and sources it to the right, at the full 40GB/s bandwidth. Additionally, it sports four 8-lane PCIe Gen 3 links on the front panel that allows up to 25.6GB/s data transfers to or from an external host computer or RAID array for continuous streaming.

Single ADC plus Single DP Module Configuration

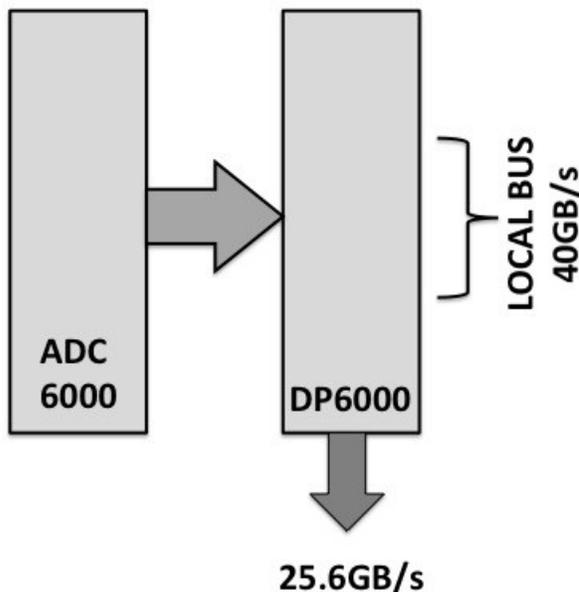


Figure 2. Each ADC 6000 module can generate 40GB/s, whether from single or multiple channels. This may be streamed at full rate to the adjacent module to the right, in this case the DP6000. The DP6000 may process it digitally, or stream it to an external host or RAID system up to 25.6GB/s. It may also stream data at 40GB/s right to another module to its right.

If the full 40GB/s needs to be streamed off-board, two DP 6000 are placed adjacent to each other, for an aggregate bandwidth of over 50GB/s. This is achieved by the DP 6000 dividing the incoming 40GB/s stream into two 20GB/s streams- and sending one out to the PCIe links on its faceplate, and sending the other to the adjacent DP6000, which directs that stream to its PCIe ports.

Streaming to RAID at full 40GB/s

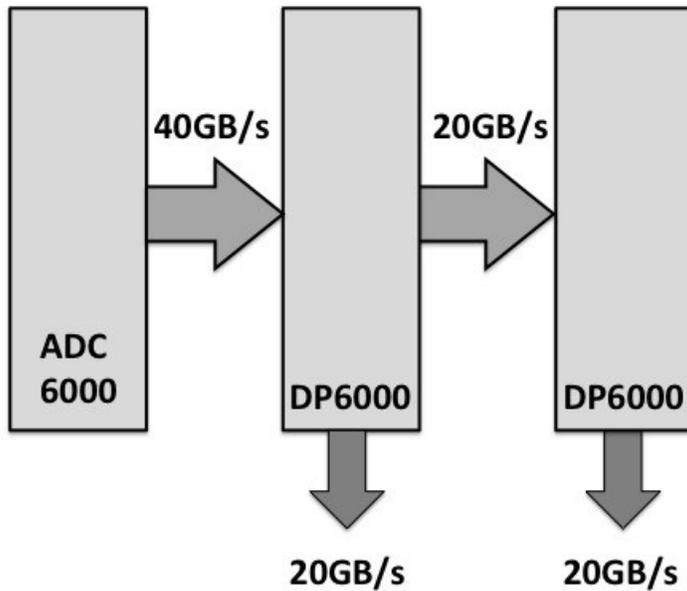


Figure 3. Since each DP6000 module is limited to 25.6GB/s externally, two may be placed in adjacent slots to achieve full streaming bandwidth to an external device. In this configuration the full 40GB/s is streamed to the first DP6000, which sends half the samples to the external RAID system, and half to the DP6000 on its right. That DP6000 streams that remaining 20GB/s to another RAID system. The data from the two RAID systems are combined for a full 40GB/s.

The DP 6000 is useful in its own right, even without connecting to an external RAID or host computer. Each module can perform fast real-time digital processing or real-time capture into its 64GB of memory. Adding more modules essentially increases the number of FPGAs processing the same data stream, or expands the amount of real time memory. Typical applications include user defined signal processing, filtering, and triggering. Of particular interest is the ability to trigger on the data, or some mathematical element of the data.

In any of the figures, multiples of digitizer modules, digital processors, or waveform generators may be deployed. These alternatives show the powerful flexibility the local bus architecture. As long as any one link may be constrained to 40GB/s, there are nearly an infinite number of combinations of digitizers, DP modules, and external PCs or RAID systems that may be configured. While the figures show single instrument sets where modules communicate on their left and right, the local bus architecture allows multiple adjacent instrument sets, operating independently. For example, Figure 2 shows a two-module set of a digitizer and a processor module; that pair may be replicated again to its right, performing a completely different function.

Future Capabilities

The digitizer and digital processor modules show some of the breakthrough capability promised by AXIe, and the local bus in particular. As noted earlier, the AXIe standard merely specifies the backplane paths for the local bus, not the particular semiconductor technology, speed, or protocol. This allows AXIe local bus speeds to grow with Moore's Law. Doubling the device speed, for example, allows 80GB/s data transfers on each local bus link. While the examples showed digitizers, the architecture is equally applicable to AXIe arbitrary waveform generators deploying the local bus. In this case, memory, data processing and massive external waveform storage may all be deployed to drive one or more wide-bandwidth arbitrary waveform generators.

Waveform Generators With AXIe Local Bus

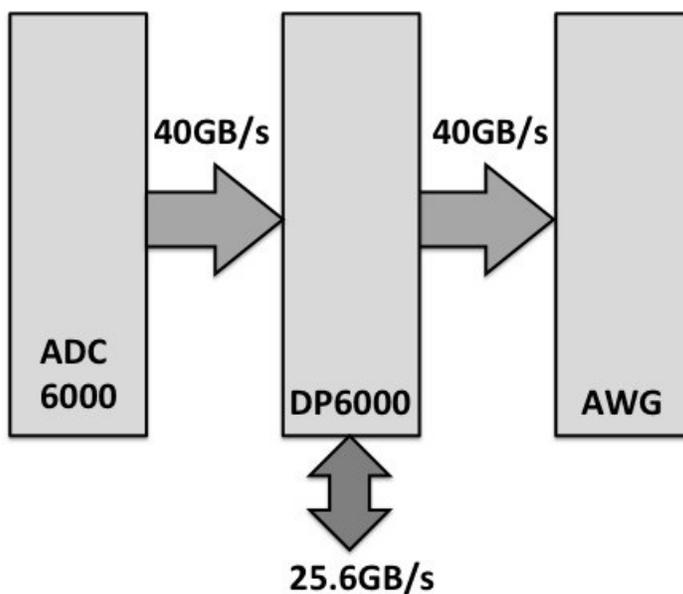


Figure 4. The local bus architecture works equally as well with arbitrary waveform generators. In this figure, a hypothetical AWG is placed in a slot to the right of the DP6000. It may have one or more output channels, but can stream data coming from its left as long as the aggregate rate is $\leq 40\text{GB/s}$.

This data may be a processed digitized stream, or it may be streamed from an external RAID system in real time.

It should be noted that the DP6000 could also be used in non-test applications as a parallel processing block, linked to hosts via its Gen 3 PCIe links. One or more may be deployed in high computational applications, including real time acceleration of digital signal processing, simulations, or databases.

Summary

AXIe delivers the board area, power, cooling and tight timing synchronization required by very high performance digital instrumentation and data converters. With the addition of the AXIe local bus, AXIe systems can now deploy real time streaming and digital processing performance well beyond traditional techniques. These features enable new applications in aerospace, defense, and high-energy physics. The unique local bus topology allows this to be accomplished in an open-system architecture that allows new levels of flexibility and scalability. Recent products from Guzik Test and Measurement show that these breakthrough performance levels may be achieved using today's technologies.

