AXIe Local Bus Speed Achieves Record 80 GB/s

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One of the unique aspects of AXIe is the local bus. As reported back in the March 2013 AXIe Newsletter, the local bus is a unique bus structure that brings a lot of hidden benefits.

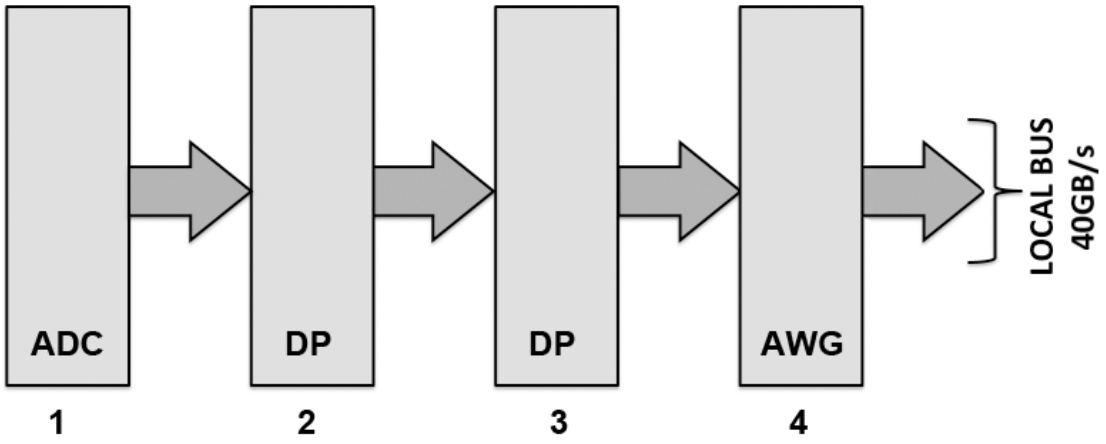


Figure 1. The diagram shows the local bus topology. It is a segmented bus that connects only between adjacent slots. A left to right flow allows very high speed streaming and independent use of each between vendors and applications.

Local buses are a set of short copper segments that connect pins between adjacent slots. This is why they are called "local" buses. For example, the right side of slot 2 is connected to the left side of slot 3. Then the right side of slot 3 is connected to the left side of slot 4, and so forth. Because the copper path lengths are short, only a few centimeters, very high-speed signals can be routed from slot to slot. Local buses enable high-speed private communication between related modules of an instrument set. Since the local bus begins and ends between the modules of an instrument set, another set of modules may use their local buses completely differently. This way, instrument sets from different vendors may co-exist in the same chassis, each exploiting the unique capabilities of the local bus. Readers are advised to read the complete March article for deeper understanding of the local bus.

A very common application is streaming of digitized data from one module to another, such as from one or more digitizers to a digital processing module. The Guzik family of digitizers was highlighted as examples in March, each capable of streaming at full sampling speed up to 40GB/s with 8-bit resolution. The large "B" is for bytes- that's bit rate of 320Gb/s with 8b/10b encoding scheme. Since each link is independent of the others, the aggregate rate increases with the number of slots.

Since the local bus is fundamentally defined as copper paths, there is no bandwidth limit imposed by the AXIe standard itself. In theory, local bus speed can increase with serial bus technology, such as drivers, receivers and connectors. The new Guzik DP 6000 Digital Processor Module is a single-slot AXIe module that was designed for enhanced local bus performance.

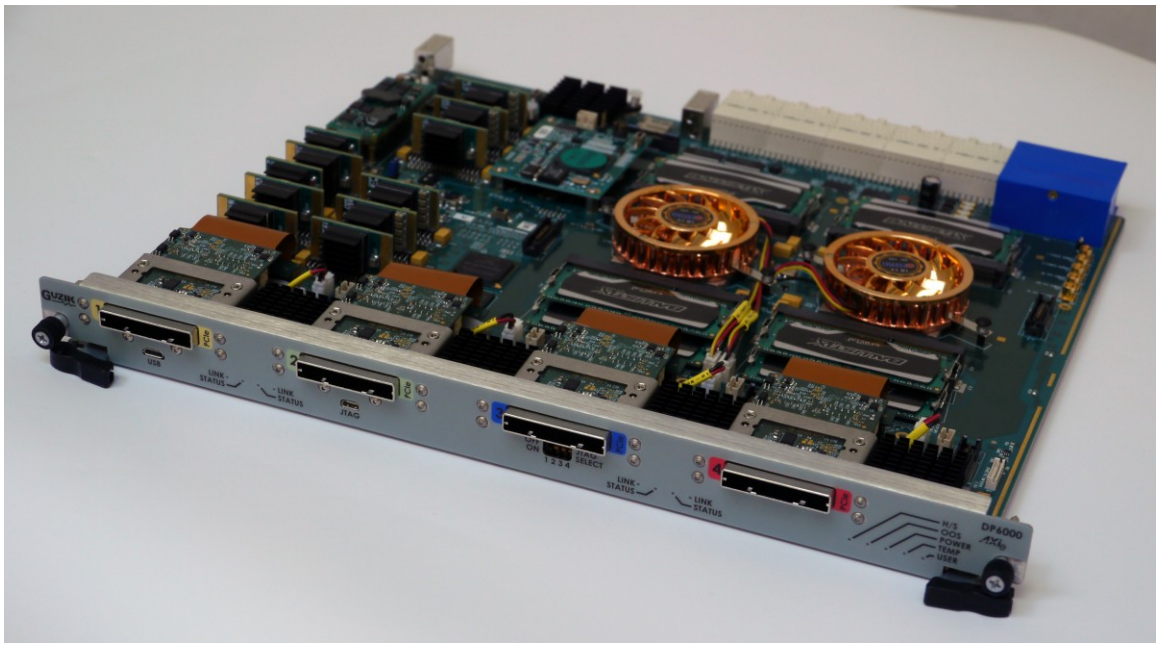
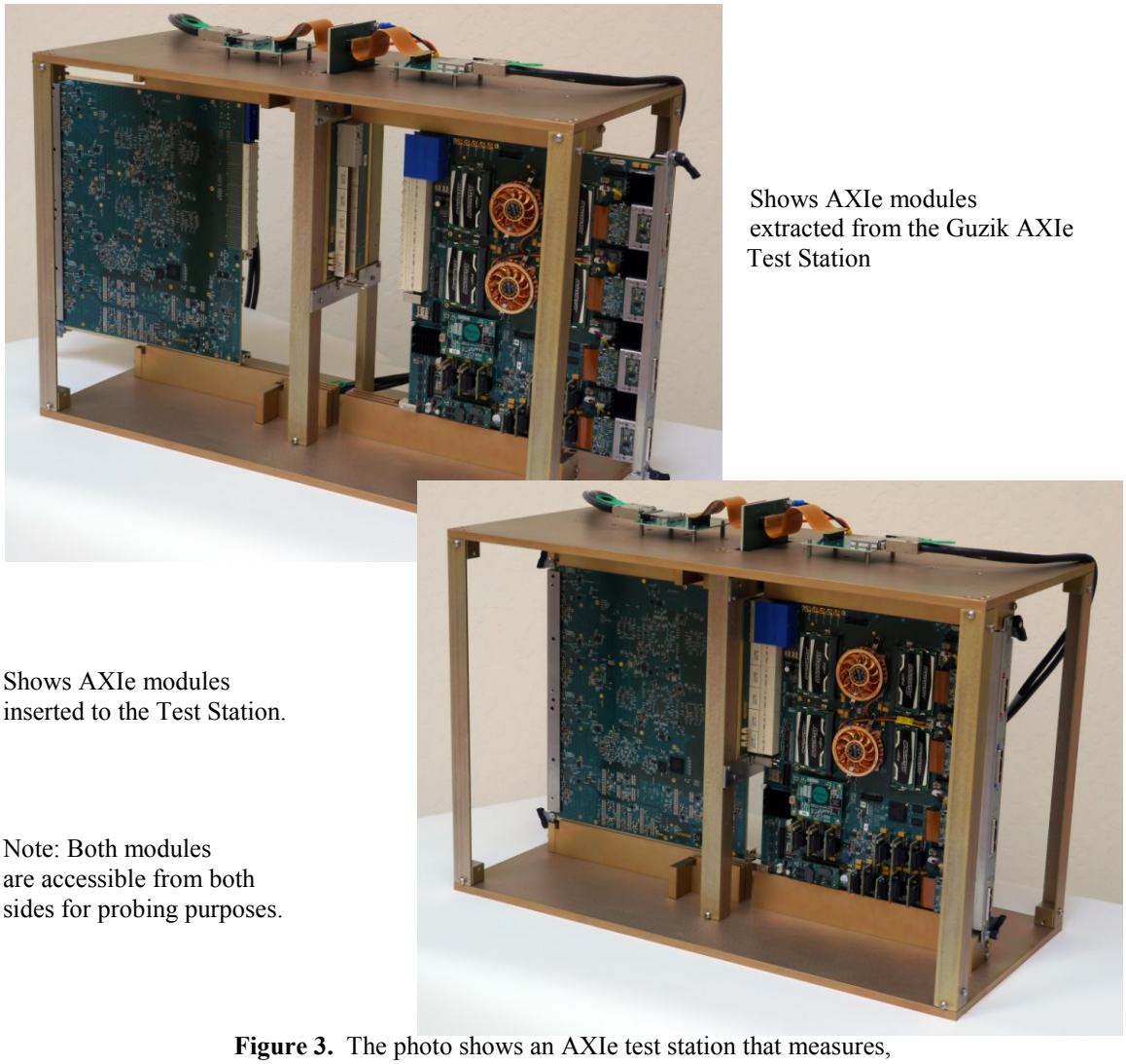


Figure 2. The Guzik DP 6000 Digital Processing Module hosts two large user-configurable Altera Stratix V FPGAs, each delivering 3,550 multipliers and 583,000 logic elements, and includes 64GB of on-board memory.

The DP 6000 highlights a number of the advantages of the AXIe local bus architecture. Like the digitizers, it accepts data from the left, and sources it to the right. Altera Stratix V FPGAs deliver powerful digital processing capability, and multiple DP 6000 can be linked together using the local bus. Additionally, each supports four 8-lane PCIe Gen 3 links on the front panel that allows up to 25.6GB/s data transfers to or from an external host computer or RAID array for continuous streaming.

Guzik has recently performed local bus performance testing on the AXIe DP 6000:



Shows AXIe modules extracted from the Guzik AXIe Test Station

Shows AXIe modules inserted to the Test Station.

Note: Both modules are accessible from both sides for probing purposes.

Figure 3. The photo shows an AXIe test station that measures, among other things, local bus performance.

Using ERNI ZD Plus connectors, and Altera Stratix V FPGAs, Guzik measured local bus bit rates of 11.25Gb/s per differential pair. This equates to 80 GB/s sustained streaming rate from slot to slot, equivalent to 640Gb/s using 64b/66b encoding scheme, which is supported by the new Stratix V FPGA-s.

Summary

The AXIe local bus topology delivers unique capabilities of performance and flexibility, while retaining interoperability between vendors. The previously demonstrated speed of 40GB/s was already best in class performance. The ability to achieve 80GB/s and effectively double the data-rate, shows that AXIe local bus speeds are able to scale with semiconductor performance, as predicted.