Guzik's AXIe Processor Modules Enable new Applications for T&M – and Beyond

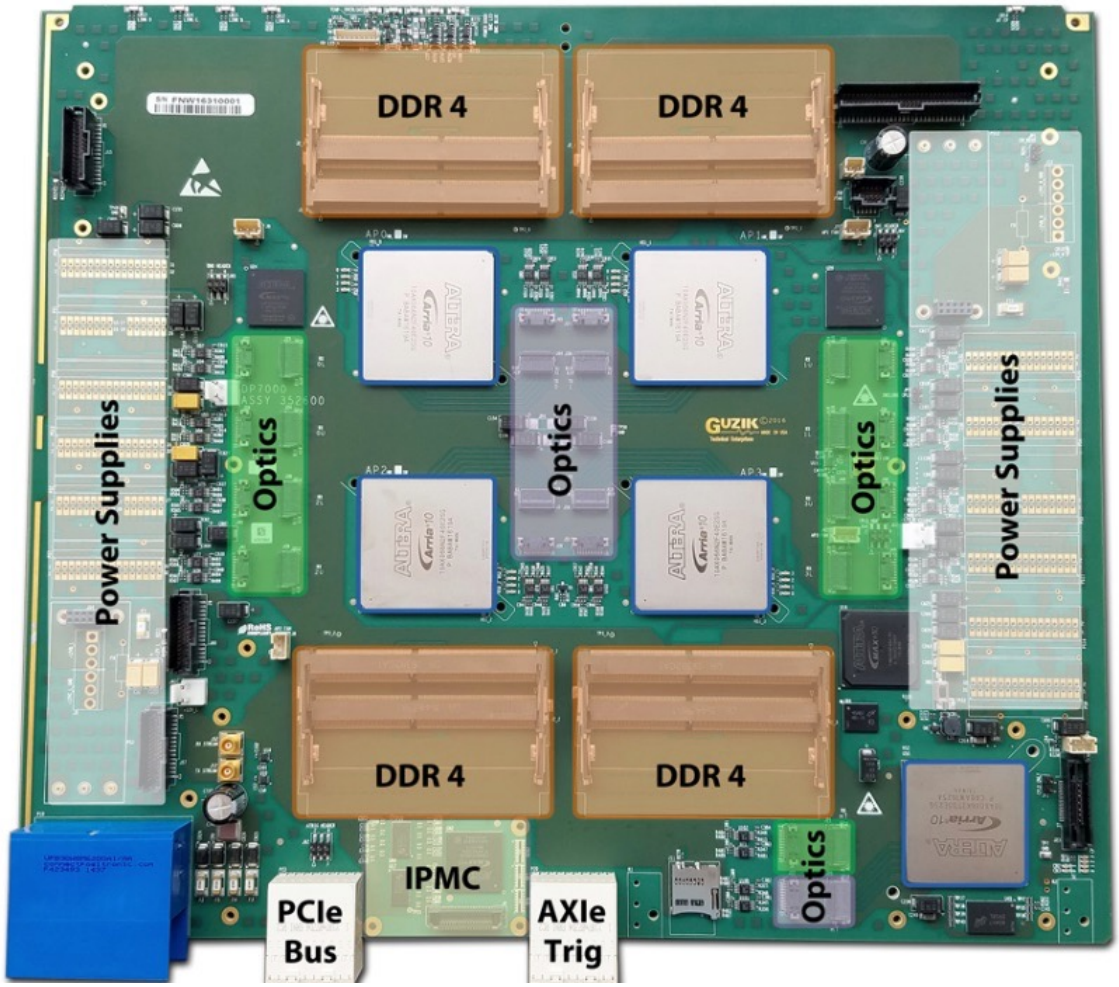
By Larry Desjardin, Modular Methods

I recently saw an announcement of two unusual AXIe-related products from Guzik Technical Enterprises, and took the opportunity to discuss these with Lauri Viitas, Director of Business Development at Guzik. Lauri described to me how Guzik was taking advantage of the AXIe architecture to offer the highest performance digital processing engines in the test and measurement industry, regardless of format, and the applications this would enable. The conversation also highlighted how difficult it would be to bring this processor, and its scalability, to any format other than AXIe.

If you are unfamiliar with Guzik, they are a supplier of disk drive test equipment and, more recently, high-performance AXIe digitizers and processing modules. I previously covered an astrochemistry application, based on AXIe, to investigate sources of life in the cosmos. The researcher, Dr. Shipman, needed a 1000x increase in measurement speed. Guzik's digitizers, with embedded onboard FPGAs for processing, were critical to meeting the speed requirement. Dr. Shipman also used an AXIe arbitrary waveform generator from Keysight Technologies.

Dr. Shipman's challenges are not unique. New test and measurement applications include 5G wireless communications and phased-array radar, where measurements must be coupled with very high performance processing to meet these very demanding applications. Being multi-channel, high-speed, and processing intensive all at the same time challenges any instrument architecture. Only modular architectures have been shown to meet this technical demand, and even then it is a technical challenge. Now, with Guzik's announcement, AXIe has taken a big leap to offer the fastest and highest bandwidth processing engines in any architecture. Let's see how.

Guzik introduced two new products, both aimed at processing. The first is the DP7000 Digital Processor, a single-slot AXIe module that now hosts the fastest signal processing in the industry. The second is the Fiber Optics Bridge Card V2, a PCIe pluggable board for a desktop computer that interfaces with the DP7000 through an optical connection.



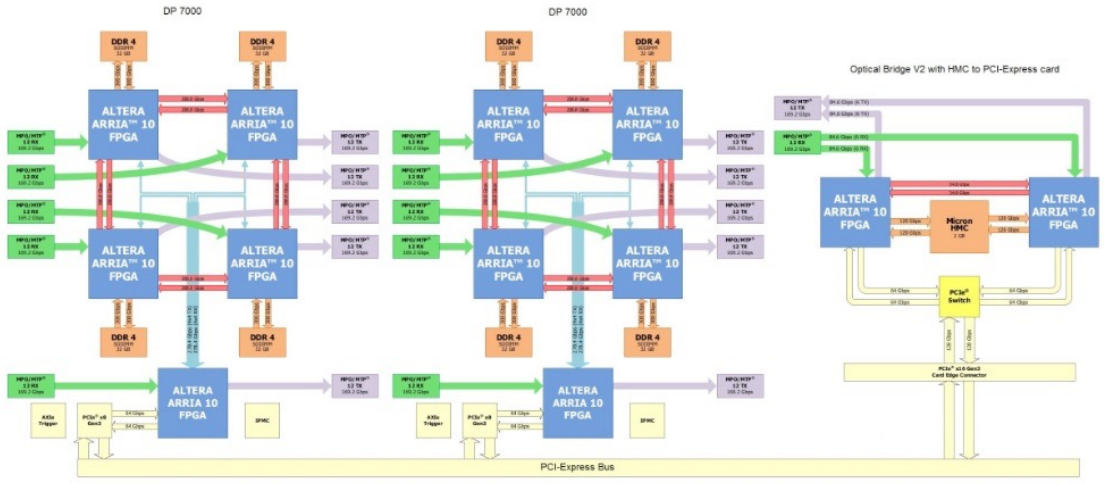
This graphic shows the layout of the Guzik DP7000. The four key FPGAs can be seen in the center, while the fifth is in the lower right. All FPGAs support direct optical connections. The board area and coplanar design, when combined with the 200W power and cooling requirements, make this a good match to AXIe. Image courtesy of Guzik.

The DP7000 hosts five Intel 10th generation FPGAs, Intel's newest 20nm FPGA offering. Intel became a major player in the FPGA space with its acquisition of Altera at the end of 2015. Each FPGA offers 1500 billion floating-point operations per second, or 1500 GFLOPS. Multiply by five, and each AXIe module is rated at 7500 GFLOPS. Four of the FPGAs are interconnected for parallel processing, with a fifth interfacing with the AXIe PCIe bus, as well as the other FPGAs. Altogether, there are over 16,000 hardware 18x19 multipliers on the module. All this processing takes power, so it is fortunate that Guzik chose AXIe, where the 200 watts needed are fueled and cooled within a single AXIe slot.

Guzik also took advantage of the new "Wide PCI Express" specification of AXIe, allowing PCIe Gen3 x8 access to the AXIe backplane.

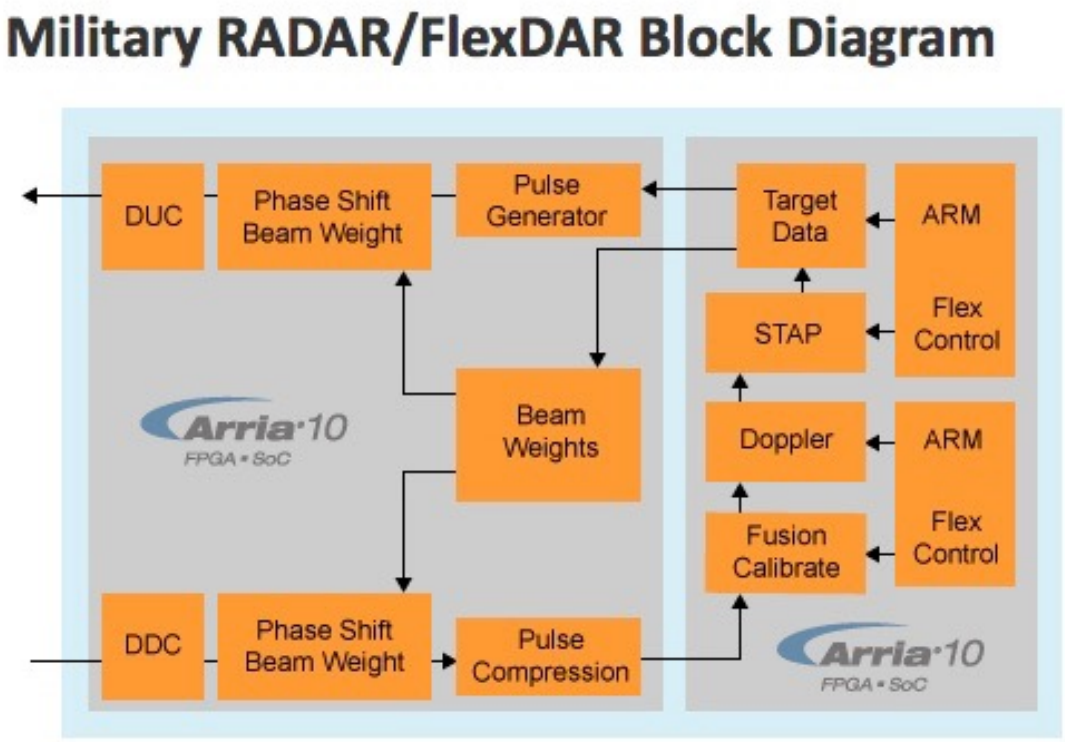
Perhaps the most architectural interesting aspect of the DP7000, is that optical interconnects are used to expand the system to multiple modules, just in case 7.5 Tera FLOPS of processing power isn't enough. Each FPGA has a dedicated optical connection on the front panel that enables 160 Gbit/s (or 20GByte/s second if you prefer byte rates) transmissions into and out of that FPGA. That's a total of 800Gb/s of real-time bidirectional throughput. Guzik actually rates the speed at 169 Gbit/s each, but I've de-rated for overhead and coding. These are easy to use optical connectors and cables that allow a user to arbitrarily connect processing elements together regardless of their physical location. The modules don't have to be adjacent to work together; they can be 100 meters apart if desired. This is convenient if you wish to separate acquisition from processing. It also avoids the nasty signal integrity and EMI issues if this is done via electrical methods.

So how do you use this? This is where the FOBC (Fiber Optic Bridge Card) comes in. It is a pluggable PCI Express card for desktops. It has a PCIe Gen3 x16 interface to the computer motherboard, two Intel 10th generation FPGAs, a Hybrid Memory Cube with 200Gbit/s connection, and a similar 160 Gbit/s bi-directional optical connection for interfacing to the DP7000. The figure below shows the data path options when two DP7000s are matched with one FOBC.



The image above shows two AXIe DP7000 signal processors (to the left) with one fiber optic bridge card (to the right) in a typical configuration. Green represents 160Gbit/s optical receivers, lavender represents similar optical transmitters, and light yellow represents the PCIe bus in AXIe and desktop controllers. Image courtesy of Guzik, and can be found on their website.

At this point you can see the scalable processing power this architecture has. Let's look at applications. The diagram below looks at the typical block diagram of a phased-array radar system.



The figure above shows the block diagram of a typical phased array RADAR system. Image courtesy of Intel.

Without going through all the details, the front ends are going digital. There is some degree of analog up and down conversion to get to the spectrum of interest, but much of the action is now in the digital domain, with digital up and down converters. Each element of the antenna is driven by a signal with a particular beam weight, phase and amplitude differences, which result in two dimensional beam steering through constructive and destructive interference. There's much more than that, as Doppler effects are calculated compensate for the object of interest.

In summary, it is a processing intensive application. Test equipment can be used to test these designs, but they also face similar, and challenging, architectural constraints. Here's where scalable processing power, such as that in the DP7000, comes in. Interestingly enough, the problem is symmetrical. An architecture that can adequately test the design may also be able to prototype it. This expands the test and measurement market to prototyping.

In my discussions with Lauri, he indicated that Guzik has been granted a US patent, number 9,148,162, “Digital down converter with equalization”. Reading through the patent, Guzik proposes a digital math scheme that reduces the number of multiplies needed to perform DDC (digital down conversion) combined with equalization. With this, DDC and equalization schemes fit tidily into FPGAs.

My point in all of this is that Guzik has chosen an architecture that can be used just as easily in prototyping or final system integration as in testing. I don’t know any architecture that has the processing power to match this, especially when one can simply add as many modules as necessary. The AXIe architecture, with its large board format and well matched power and cooling capabilities is a key enabler. But there is one catch.

While many of today’s signals can be passed via the embedded PCIe busses from the data converters to the processing modules with the current PCIe Gen 3 architecture, we’re running out of headroom to do so. The data bandwidths are increasing. The obvious weak link in all this is the finite bandwidths of the electrical busses, such as PCIe, versus the optical busses that can transmit much more. Guzik is offering nearly 100GByte of bandwidth between their DSP modules via optical, but only 8Gbyte/s via the PCIe path, the only interface to instrument modules. The obvious tact is to create instruments that also use optical interfaces.

When pressed on this, Lauri would only say, “stay tuned.” Read into that what you wish.