AXIe Consortium Introduces Wide PCI Express for AXIe

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This month, the AXIe Consortium released a specification named "Wide PCIe", expanding the lane width, and associated data throughput, to or from an AXIe module. Previously, all PCIe (PCI Express) fabrics were a maximum of four lanes wide. Wide PCIe allows a module to support up to either 8 or 16 lanes of PCIe in each direction. Wide PCIe is a preliminary specification posted on the AXIe Consortium website in slide format. It will be formally integrated into the next revision of the AXIe-1 specification.

The "Wide PCIe" specification is straightforward. The AXIe Consortium had previously reserved pins at each slot for expanding the PCIe lane width. In the parlance of AXIe and AdvancedTCA, modules were only allowed to use Fabric Channel 1, a four-lane PCIe bus, but other fabric channels were reserved. The new specification now allows Fiber Channels 2, 3, and 4 to transport data as well, allowing up to 16 lanes of transit in each direction.

The specification preserves backwards compatibility. That is, a module designed for four lanes will operate in a chassis designed for 8 or 16, though only four lanes will be enabled. Similarly, a module designed for 8 or 16 lanes will operate in a chassis offering only four lanes. Again, only four lanes would be enabled. When the module and chassis each support 8 or 16 lanes, the higher bandwidth of Wide PCIe can be achieved.

While Gen 2 PCIe fabric is commonplace today in AXIe, Gen 3 can be supported as modules and chassis become available. Depending on the speed of the PCIe fabric, the following theoretical speeds, in GByte/second, can be achieved:

GByte/s	Gen 2	Gen 3	
PCIe x1 GBps	0.50	0.98	
PCIe x4 GBps	2.00	3.94	<-- Previous top speeds available
PCIe x8 GBps	4.00	7.87	
PCIe x16 GBps	8.00	15.74	<-- New speeds available due to Wide PCIe

Essentially, each doubling of lane width equates to a generation jump in PCIe speeds. It should also be noted that the nominal speeds above should be de-rated 20% for real world implementations.

The one restriction to the wider PCIe deployment is that it is focused on integrated chassis, where the system module is embedded within the chassis. This is the most common AXIe chassis implementation. Typically, a Cable PCIe link then connects from the embedded system module within the chassis to the external test system controller. However, the test system controller may be embedded as well.

The consortium will also be addressing techniques for Wide PCIe deployment in non-integrated chassis in the future.

By adopting Wide PCIe, the AXIe community has increased the PCIe bandwidth four-fold, bringing it to the neighborhood of 10GByte/second. Combined with the large format module size, high power and cooling, precision timing, and high performance local bus, AXIe continues to define a platform for very high performance modular instrumentation.