

AXIe: AdvancedTCA[®] Extensions for Instrumentation and Test

July 1, 2010

 AEROFLEX



Agilent Technologies



Giga-tronics



testevolution.com



ADLINK
TECHNOLOGY INC.




Test and Measurement



Tyco Electronics

Copyright © 2009 AXIe Consortium, Inc.

* AdvancedTCA is a registered trademark of the PCI Industrial Computer Manufacturers Group (PICMG)



AXIe Specifications: What and Why

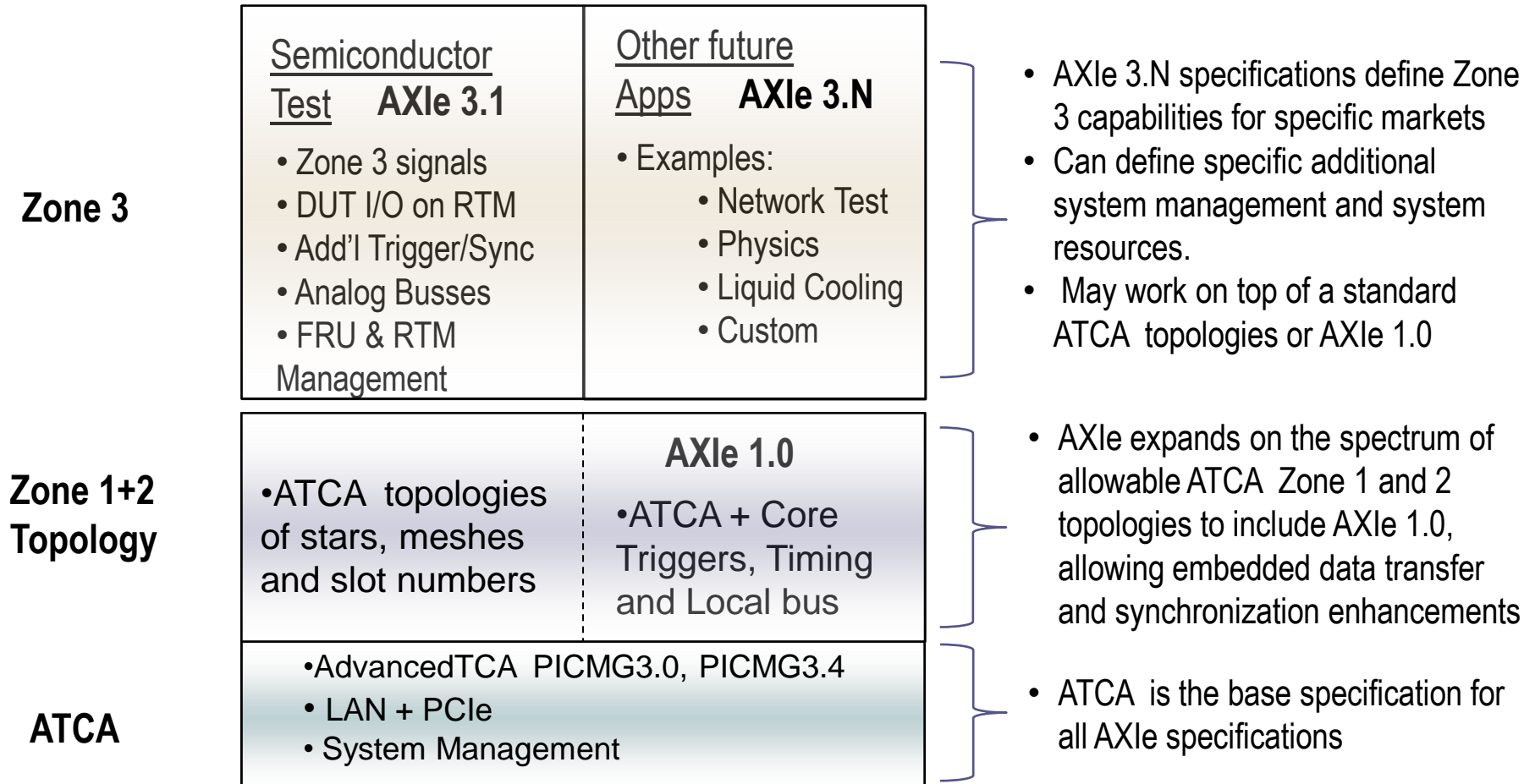
- **What is it?**
 - A family of next-generation, open specifications that extends Advanced Telecom Computing Architecture (AdvancedTCA[®]) for general purpose and semiconductor test
- **Why another modular test standard?**
 - Higher performance per rack inch
 - Greater scalability
 - Integrates easily with PXI, LXI and IVI
 - More modularity, more flexibility, higher speeds => addresses a range of platforms
 - ATE Systems, rack-and-stack modular, bench top, module plug-ins
 - Significant reduction of development and unit costs

Why AdvancedTCA as a foundation?

- **AdvancedTCA PICMG® 3.0 Specification:** *proven* open system architecture
- **Large board size**
 - Ideal for high performance instrumentation
 - Board size matches that of planar instrument design
- **Rack space efficiency**
 - Horizontal and vertical configurations
- **Scalability**
 - 1 slot to 16 slots, 1 Chassis to many, PXI/PCI adapters
- **Ideal for high power applications**
 - Single rail power management and robust cooling
- **Virtual LXI and PXI**
 - Base fabric support of LAN, data fabric support of PCIe
- **Robust system management**
 - Intelligent Platform Management Interface (IPMI) enables both single chassis and multi-chassis system control functions
- **Extensions** for I/O, custom backplanes, liquid cooling

AXIe Specification Structure

AXIe is a scalable family of specifications allowing a portfolio of applications.



AXIe 1.0 and 3.1 Features

| Feature | 1.0 | 3.1 |
|--|-----|-----|
| PCIe & LAN Hubs | x | |
| Local Bus | x | |
| Trigger Bus (TRIG) | x | |
| Frequency Reference (CLK100) & Sync (SYNC) | x | |
| Star Trigger (STRIG) | x | |
| Bidirectional DSTAR (4) | | x |
| User Defined Synchronization Signals | | x |
| Load Board Support | | x |
| Field Calibration Support | | x |

AXIe leverages ATCA

AXIe

AdvancedTCA

- AdvancedTCA specific extensions
- IPMI and resource management
- Timing and Sync
- Zone 3 configurations

...draws from and works with existing instrument standards

PXI

- Virtual PXIe instruments
- PCIe communication

IVI

- Standard drivers work in all Application Development Environments
- VISA specifications

LXI

- Virtual LXI instruments
- LAN communication

High scalability of AXIe

14 slot Vertical



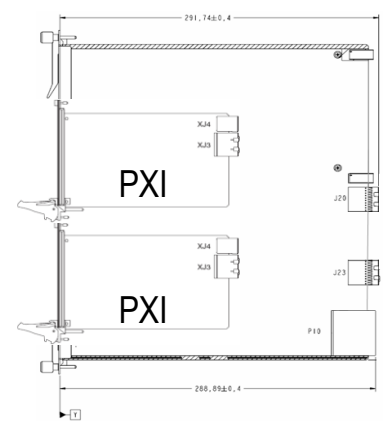
n U Horizontal



1U



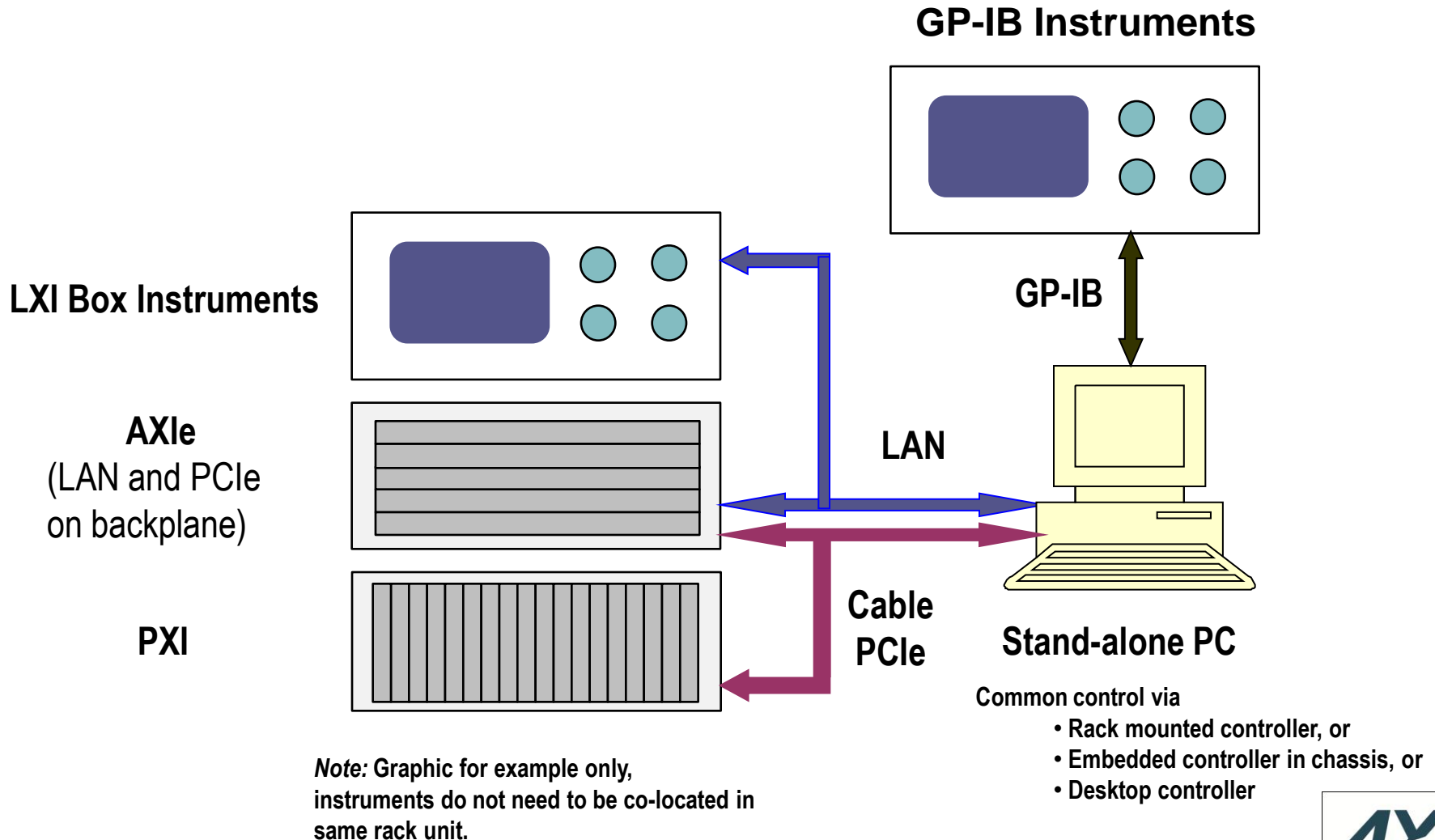
Specialty instrument with AXIe module



PXI carrier module



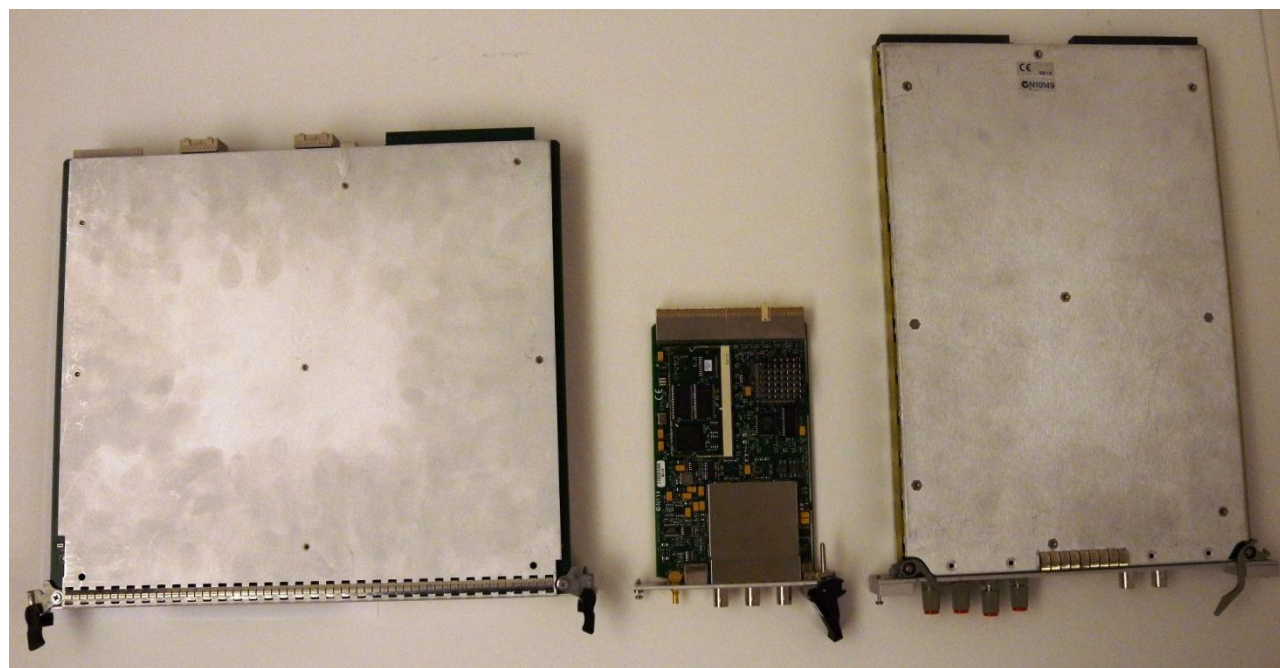
AXIe integration with Rack and Stack



Module size comparisons

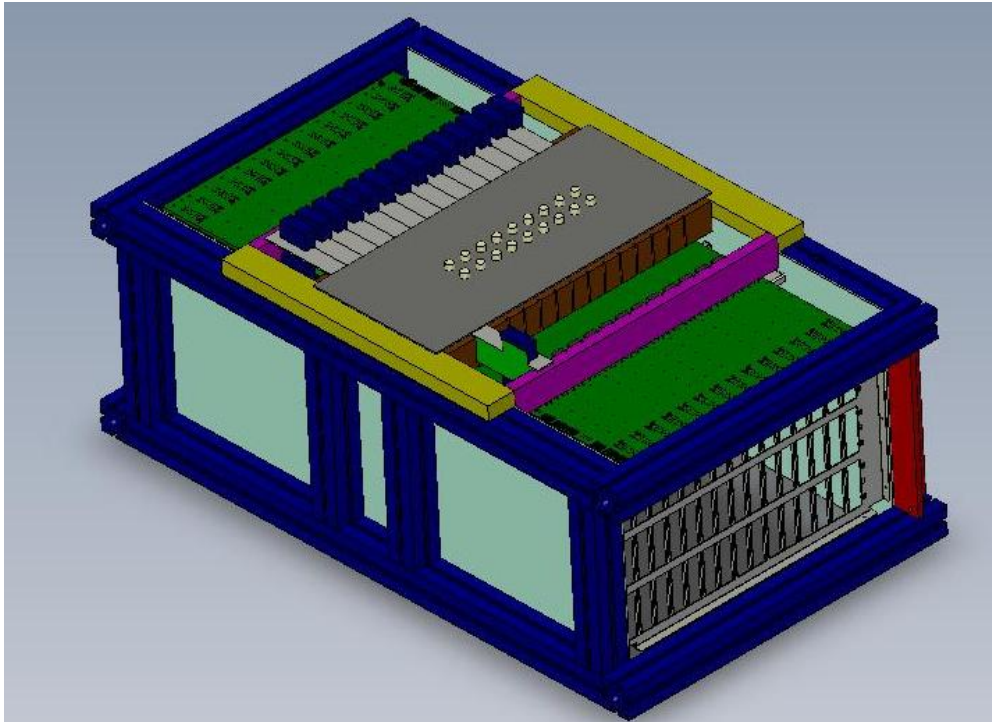


3U-PXI VXI AXIe



AXIe 3U-PXI VXI

AXIe integration in Semiconductor Test



Note: Graphic for example only.

- Scalable combinations of ATCA, AXIe and PXI chassis
- Zone 3 Extensions for digital synchronization DUT I/O, and other ATE system resources

Summary

- **Extending AdvancedTCA**
 - AXIe is based on AdvancedTCA with extensions for instrumentation and test.
- **General Purpose (1.0) & Semiconductor Test (3.1)**
 - AXIe will have a base architecture specification of AXIe 1.0 for general instrumentation, and a Zone 3 specification AXIe 3.1 for semiconductor test.
- **More Performance, Scalability, Flexibility**
 - AXIe delivers higher performance in a flexible, scalable platform.
- **PXI, LXI, IVI**
 - AXIe works well with other standards, such as PXI, LXI and IVI.
- **Lower costs**
 - Enables significant reduction of development and unit costs.
- **Longevity**
 - Promises longevity due to high performance coupled with layered specifications

Specification Management

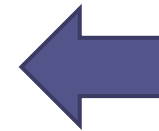
- **AXIe Consortium**
 - AXIe Consortium manages AXIe 1.0 and 3.1 specifications
 - For more information, go to www.axiestandard.org or email Bob Helsel, Executive Director at execdir@axiestandard.org
- **Potential future AXIe standard efforts**
 - Improved integration of ATCA, AXIe 1.0, and AXIe 3.1 combinations
 - AXIe 2.0 software specification
 - AXIe 3.N specifications for additional markets
 - Fully integrated PXImc
 - MicroTCA[®] derivatives for AXIe

Technical Overview Slides

- **AdvancedTCA**
- **AXIe 1.0**
- **AXIe 3.1**

Technical Overview Slides

- **AdvancedTCA**
- **AXle 1.0**
- **AXle 3.1**



Advanced Telecom
Computing Architecture

PICMG 3.0 AdvancedTCA Specification

- AdvancedTCA (Advanced Telecom Computing Architecture)
- Larger form factor cards
- Flexible power (48V) and air cooled design
- PICMG 3.4 Specification for PCIe signaling on Zone 2 Fabric
- Intelligent Platform Management Interface (IPMI)

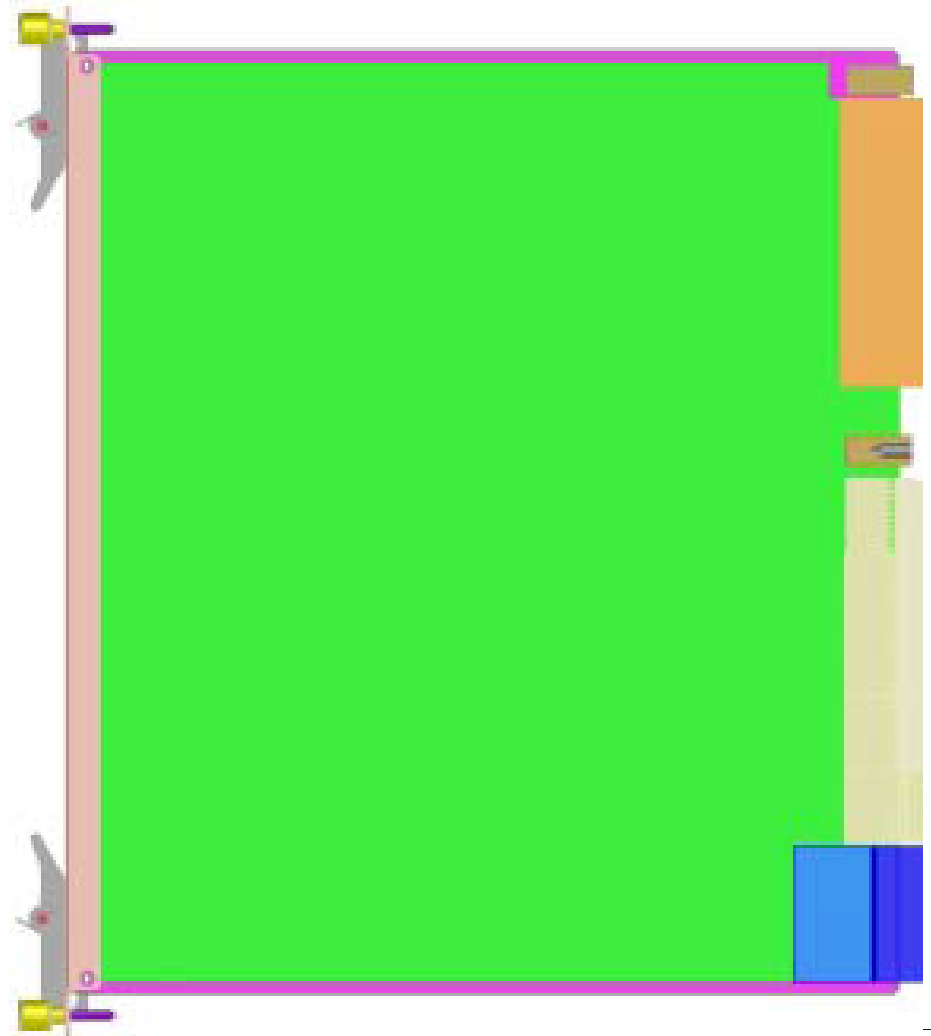
AdvancedTCA Shelf (Chassis)

- 2-16 Slot Shelf
 - 2-14 Slots in 19" Rack
- 2 Hub Slots
- 14 Node Slots
- User Zone 3 Backplane



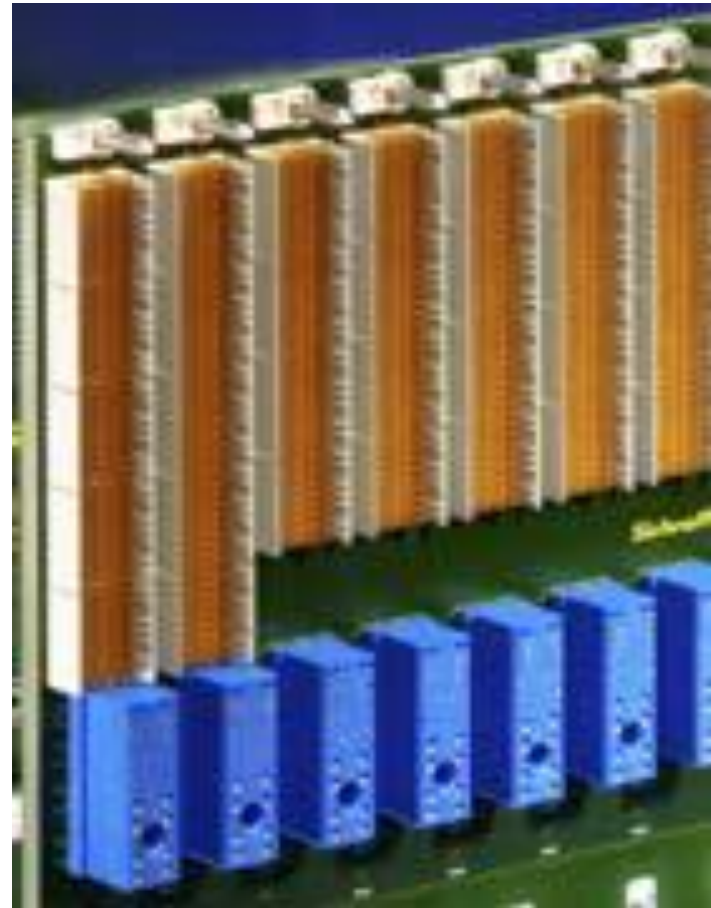
AdvancedTCA Front Boards (Modules)

- 322mm x 280mm
- >200W Power Dissipation
- 1.2 in card spacing

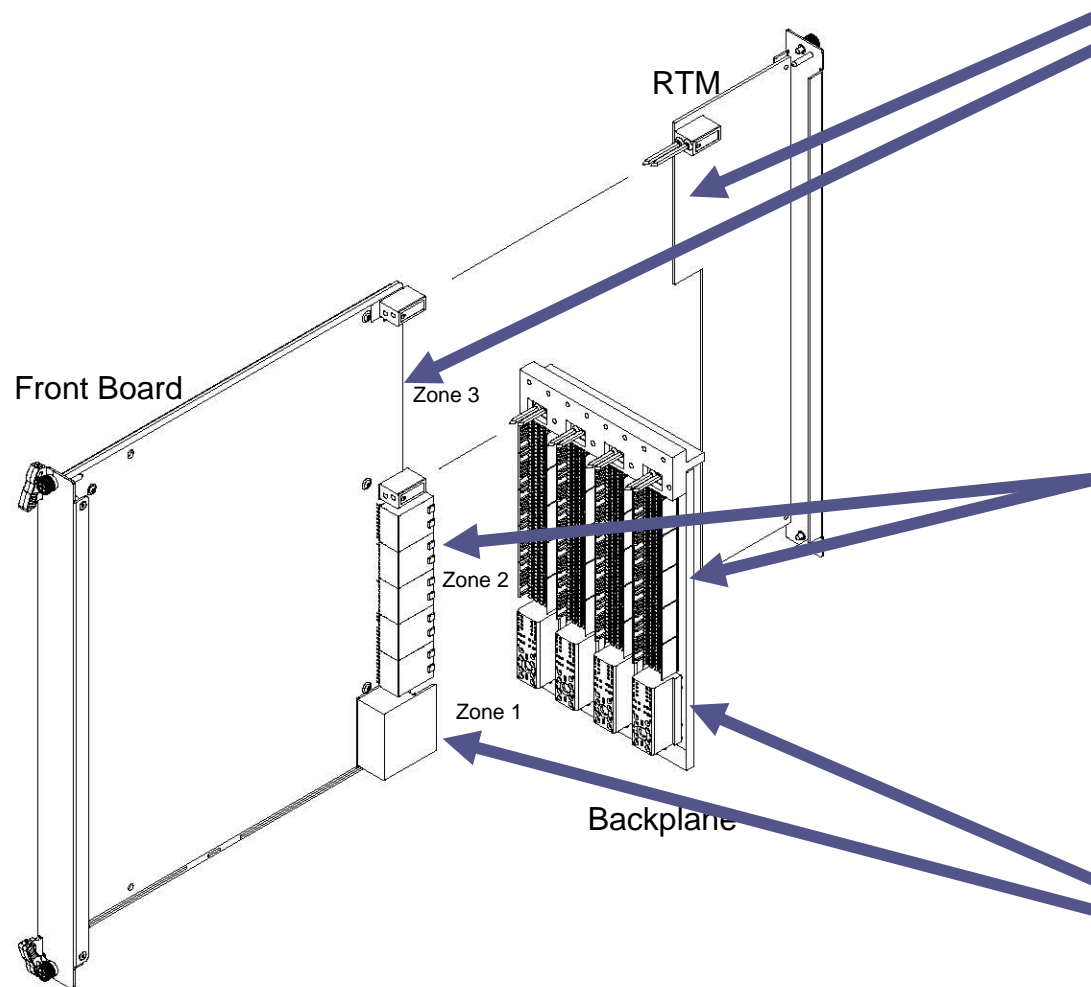


AdvancedTCA Backplanes

- Zone 2
 - Serial Fabric and Base Channels
 - Dual Star to Hub Slots
 - Reference Clocks
 - Update Channel Links
- Zone 1
 - Power
 - IPMI
 - Geographical Address
 - Telecom Analog Buses



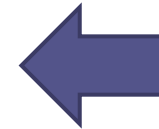
AdvancedTCA Connector summary



- ZONE 3: Rear Transition Module is an AdvancedTCA option traditionally used for I/O
- PICMG allows each slot connector to be customized
- ZONE 2: Serial fabric and reference clocks. Allows 4 lanes of PCIe
- Typical configuration is a dual star
- ZONE 1: Power and Management

Technical Overview Slides

- **AdvancedTCA**
- **AXIe 1.0**
- **AXIe 3.1**



AXIe Base Architecture Specification

AXIe 1.0 Chassis

- Logical Slot 1 (Hub 1 slot) is the AXIe System Slot
- Logical Slots 2-14 (Hub 2 and Node slots) are AXIe Instrument Slots
- Logical Slot 2 (Hub 2 slot) is also the AXIe Instrument Hub Slot
 - Fabric Channel 2 open for proprietary or future definition
- Up to 13 instrument modules in a 14 slot chassis
- Zone 3 reserved for AXIe defined extensions

AXIe 1.0 Communication and Timing

- LAN and/or PCIe connectivity to host computer
 - LAN distributed over Base Fabric
 - PCIe distributed over Data Fabric
 - PCIe reference clock distributed over FCLK star
- AXIe Core GP Timing and Triggering
 - Star CLK100 (100Mhz), Star SYNC
 - Matched length
 - Star STRIG - Matched Length
 - Trigger Bus (12 MLVDS pairs)
 - Local Bus (18 to 62 LVDS pairs from slot n to slot n+1)

AXIe 1.0 Leverages AdvancedTCA Specifications

- PICMG 3.0 AdvancedTCA Specification
- Mechanical, Power, and Intelligent Platform Management Interface (IPMI)
- Base Interface: Gigabit Ethernet LAN
- PICMG 3.4 Specification for PCIe signaling on Zone 2 Fabric

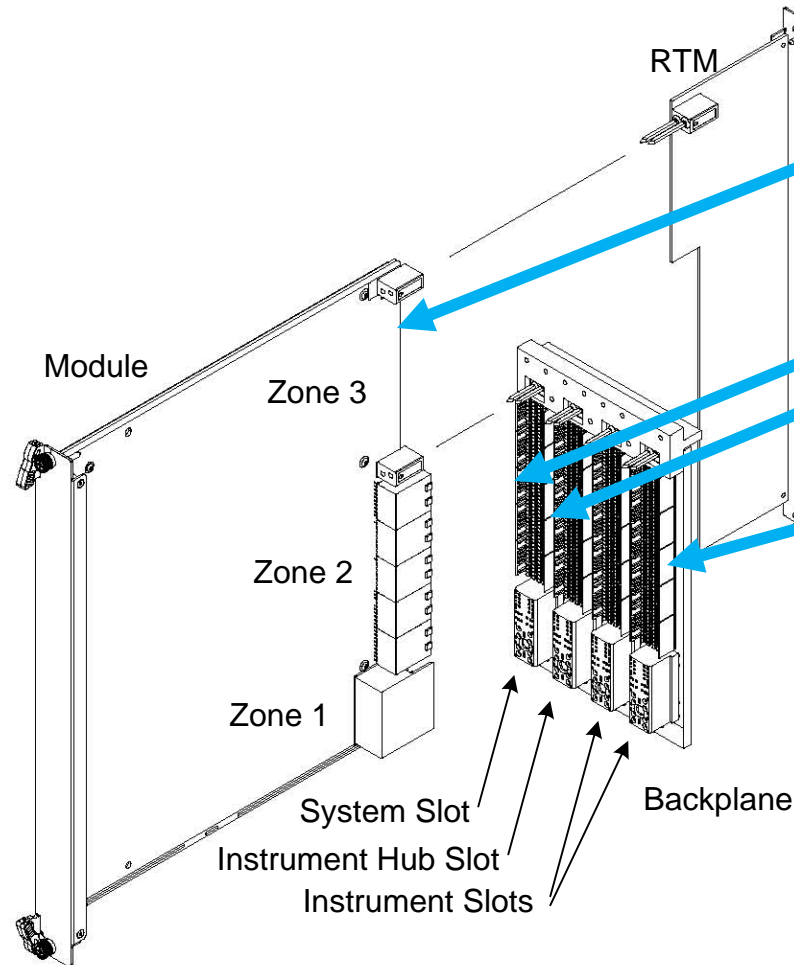
...but adds

- High speed segmented local bus between adjacent slots
 - Utilizes unused transport fabric and base channel pins for AXIe Local Bus
 - 18 high speed differential pairs per link minimum, up to 62
- Timing and Triggering
 - Synchronous and asynchronous timing and trigger lines
 - Fabric clock for PCIe reference clock distribution
 - Utilizes ATCA telecom-defined clock and Update Channel pins

Result: Powerful general purpose instrument architecture that does not impact or use Zone 3, allowing compatibility with current AdvancedTCA products and any AXIe extensions that use a defined Zone 3.

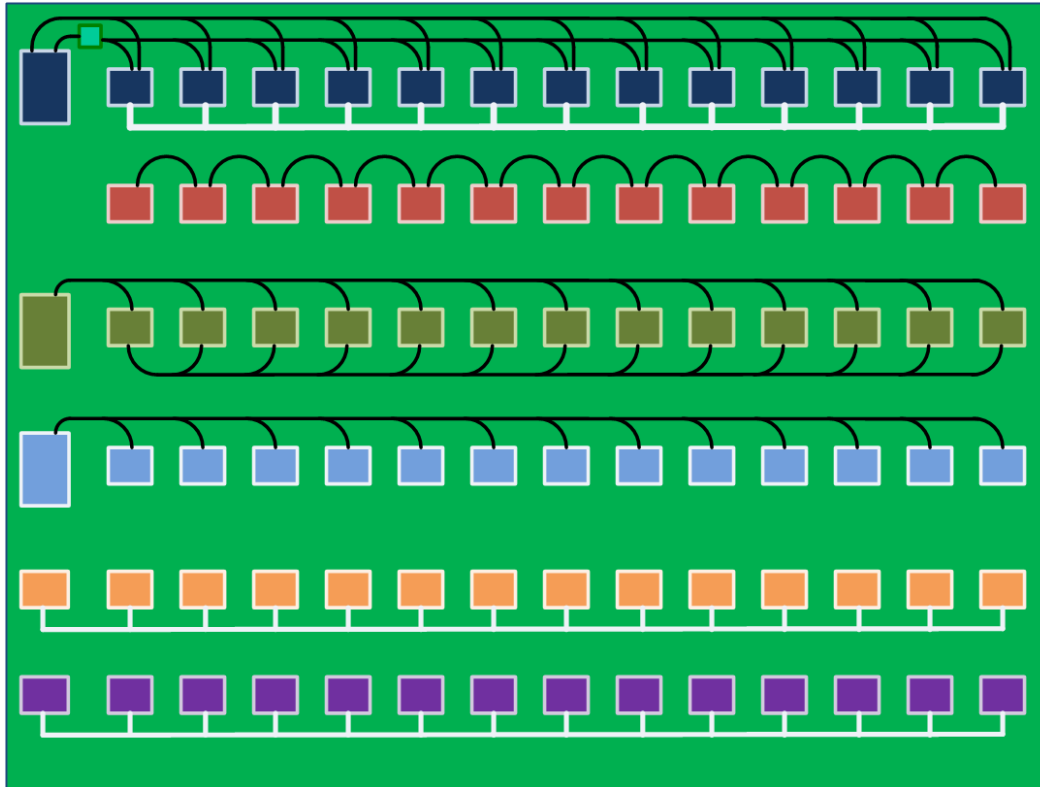


AXIe 1.0 Connector Summary



- RTM connectors and space reserved for AXIe extensions
- Utilize Dual Star fabric:
 - FC1 for PCIe
 - FC2 proprietary
- Eliminate slots 15 and 16
- Utilize Unused base and fabric pins for Local Bus
- Utilize Update Channel pins for Timing Interface and Trigger Bus

AXIe 1.0 Backplane Layout (14-slot Example)



Timing Interface: Clocks and star triggers

Trigger Bus: Parallel triggers

Local Bus: 18, 42 or 62 pairs

PCIe Data Fabric: x4 link to each slot
(Second star data vendor-defined).

1Gb Ethernet LAN

IPMB: Intelligent Platform Management Bus
used for chassis system control functions

Power Rail: (-48V)



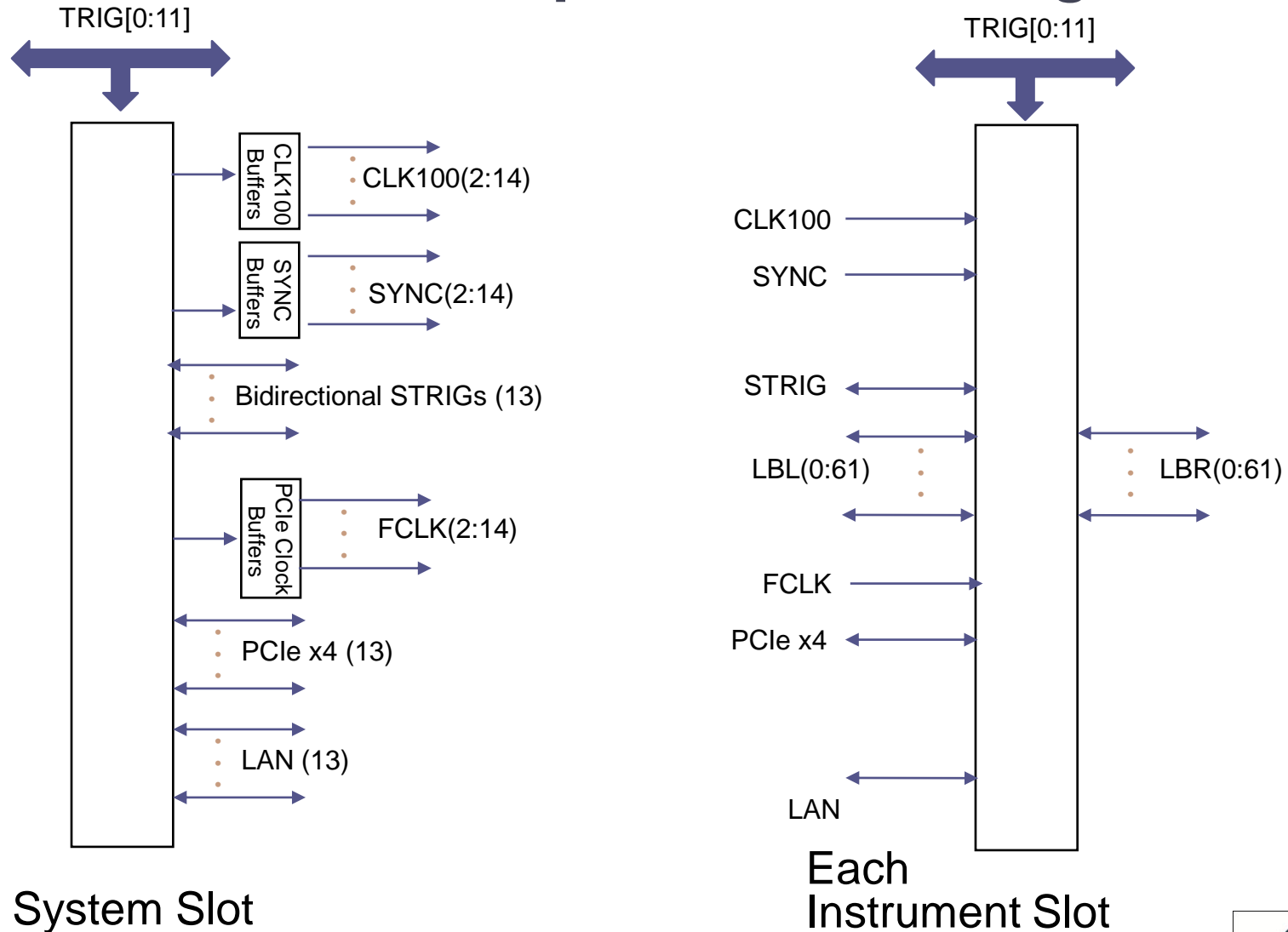
Note: System Module may be built into the chassis
Note: Graphic shows 14 slots as example only

AXIe 1.0 System Module

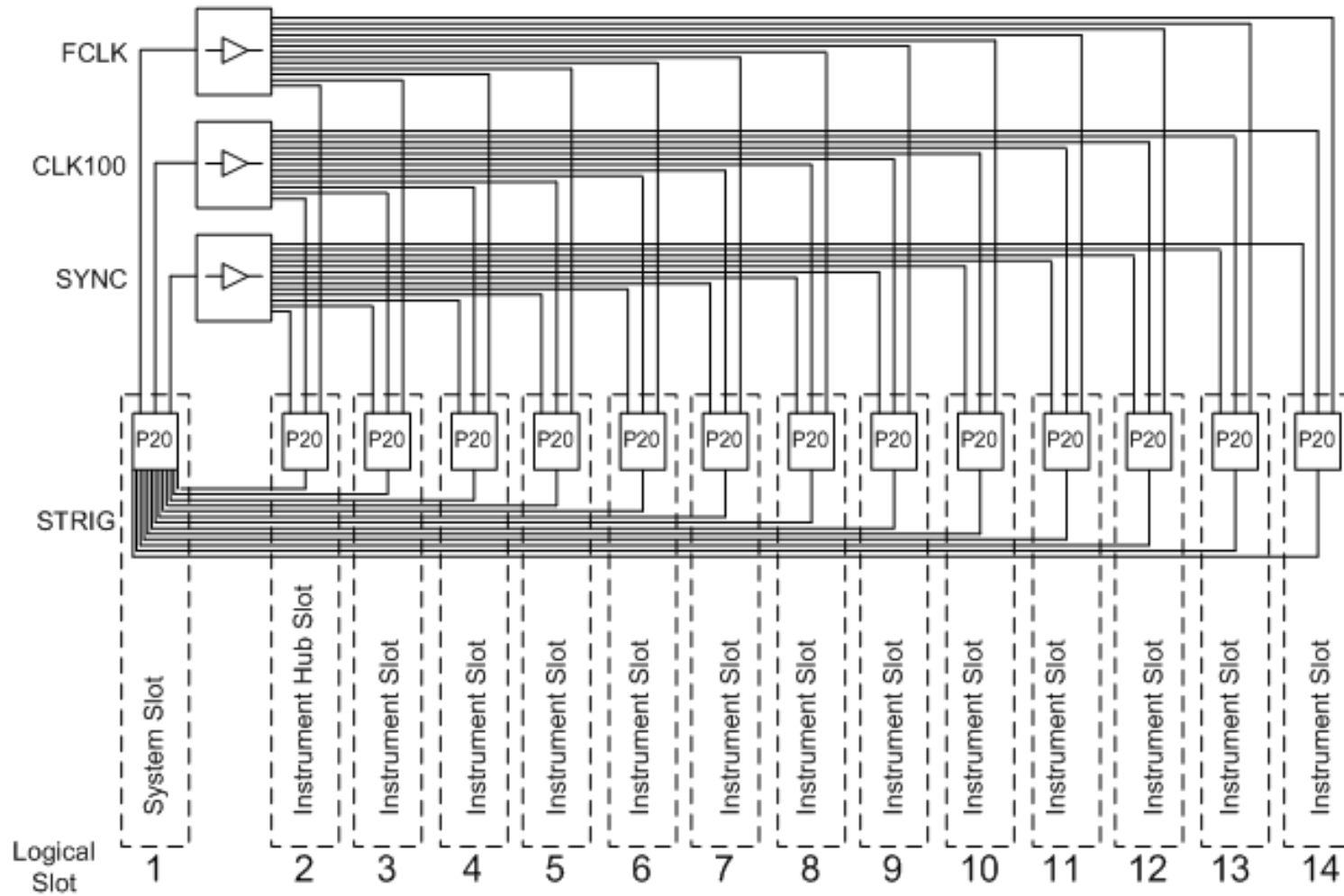
- Resides in Logical Slot 1
- Sources CLK100, SYNC, and FCLK
- Routes Star Trigger (STRIG) to Instrument Modules
- Connects to Trigger Bus
- Routes signals between TRIG, STRIG, SYNC, and external trigger connections
- Switch/Hub for LAN and PCIe



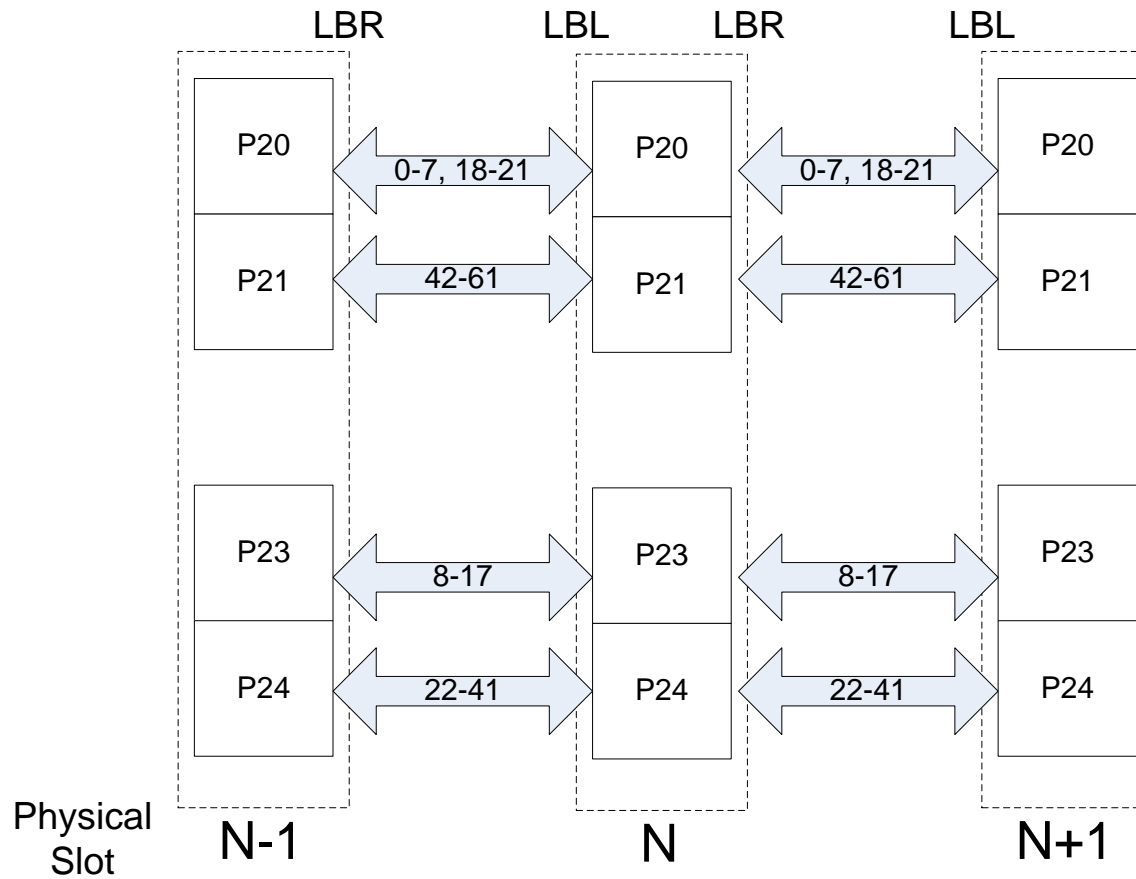
AXIe 1.0 Zone 2 Backplane Block Diagram



AXIe 1.0 Timing Interface Topology

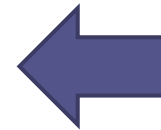


AXIe 1.0 Local Bus Topology



Technical Overview Slides

- **AdvancedTCA**
- **AXIe 1.0**
- **AXIe 3.1**



AXIe Semiconductor Test Extension

AXIe 3.1 Vision

- Create instruments, sub-systems and systems in open standard formats for semiconductor test applications
- Support both bench top Characterization and Production Automatic Test
- Standard Chassis for
 - High Speed Digital Pins
 - DC & Power Instrumentation
 - High Channel Count Instrumentation (i.e. multi-site)

AXIe 3.1 Chassis

- Defined Zone 3 Backplane
 - DUT (Device Under Test) I/O in RTM
- Layered on top of ATCA or AXIe 1.0 Zone 1 and 2 backplane
- Enhanced System Module
- Up to 15 instruments in 16 slot chassis

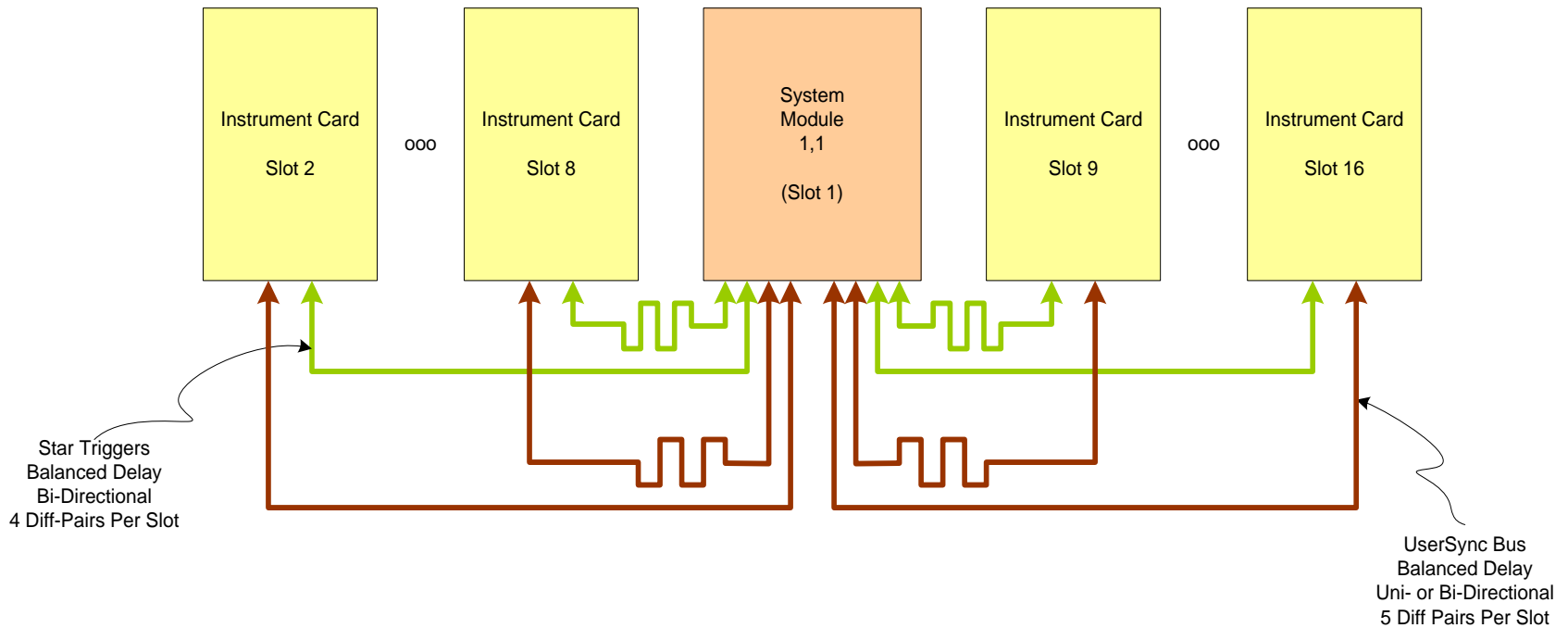
AXIe 3.1 Extensions

- Timing and Triggering Extension
 - Star Triggers
 - User-Defined Synchronization
- Load Board Support
 - DUT I/O via Rear Transition Modules
 - Load Board Configuration Management
 - Power
- Field Calibration Path
 - 4 Wire Kelvin Interface Bus
 - 1 Amp, 300 Volt Max

AXIe 3.1 Triggers

- Asynchronous Triggering
 - 4 Star Triggers from System Module to each Instrument node
 - Bi-directional Differential Terminated BLVDS
 - Matched Length
 - 5ns Min Pulse width
- Custom Synchronization: UserSync
 - 5 star-distributed signals from System Module to each Instrument node
 - Bi-directional Differential Terminated BLVDS, matched length
 - For system-defined instrument synchronization protocols

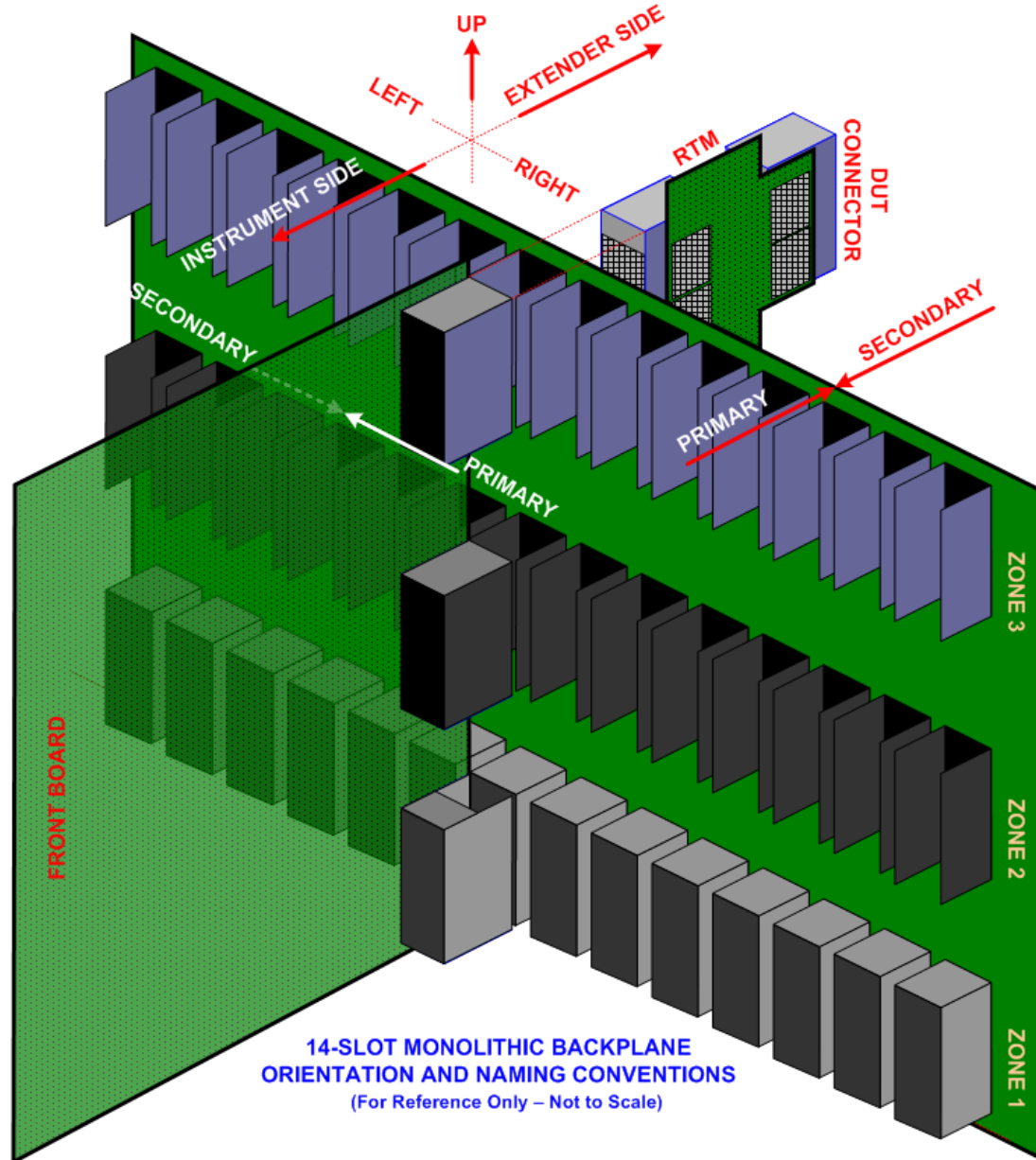
AXIe 3.1 Triggering: Up To 16 Slot Cage



AXIe 3.1 Triggering Applications

- Asynchronous
 - Instrument<->Instrument triggering for action<->status operation
 - Encoded triggers to convey information between instruments
 - One-to-many triggering for multi-site testing
 - Multi-chassis trigger support
- UserSync Bus
 - Providing specialized or tightly-timed synchronous triggers
 - Providing matched length, specialized clocks to instruments
 - Synchronizing digital and mixed-signal pins
 - Synchronizing multi-board instruments

AXIe 3.1 Backplane Layout



14-SLOT MONOLITHIC BACKPLANE
ORIENTATION AND NAMING CONVENTIONS
(For Reference Only – Not to Scale)

AXIe 3.1 System Module Slot

- Enhanced System Module Board (i.e. 3.1 SM)
- 32 DUT I/O signals
- Analog and Calibration Bus Support
- Power (+/-15, +/- 5, 48) to DUT Load Board
- I2C Bus for Load Board/Extender Card ID
- I2C Bus to control Load Board/Extender card electronics
- Hub for Point to Point Triggers to node slots
- Hub for Point to Point User-Defined Synchronization bus

AXIe 3.1 Node Slot

- 152 DUT I/O signals
- Support for active electronics in DUT signal path
 - I2C Bus for FRU information
 - I2C Bus for register access
 - Power (+ 5V)
- Four Point to Point Triggers from System Module Slot
- Five-Signal Point to Point User-Defined Synchronization Signals
- Access to Analog and Calibration Busses

Further Information

- Specifications may be downloaded from the AXIe Consortium website at www.axiestandard.org