AXIe
Wide PCIe

(***Note:*** Features now incorporated into AXIe-1.)

Preliminary Specification

AXIe Wide PCIe

- Situation
  - Current AXIe-1 specification defines 4-lane PCI Express fabric (PCIe x4) to each instrument slot.
  - This equates to 1GB/s (Gigabytes/second) nominal data throughput using Gen 1 technology, 2GB/s using Gen 2, and 4GB/s using Gen 3.
  - Wider fabrics would proportionally increase data throughput

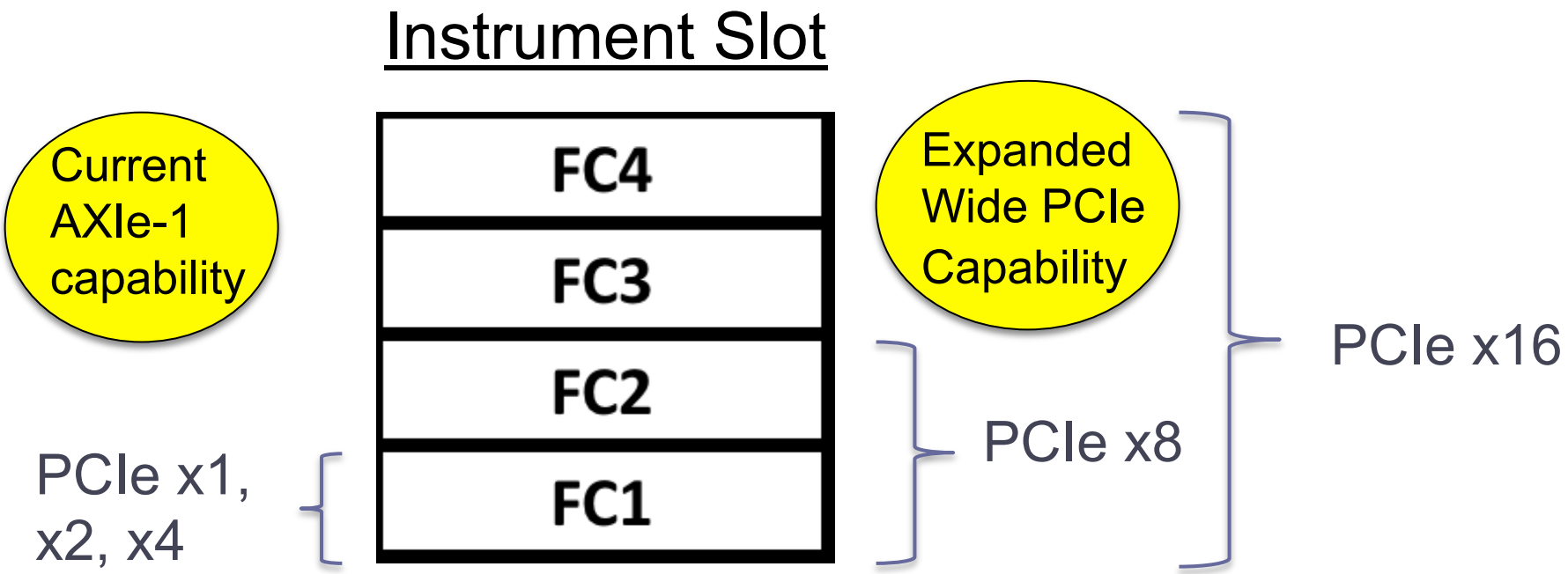
- Goals
  - Create a specification for instrument modules that allow x8 and x16 PCIe deployments

Introducing AXIe Wide PCIe

- Preliminary specification, augmenting current AXIe-1
- Will be formalized within AXIe-1 specification
- Addresses chassis and instrument modules
- Expands PCIe lane width to x8 and x16 per instrument
- Backwards compatible with current x4 AXIe products
  - Wide PCIe modules operate as x4 inside x4 chassis
  - Current x4 modules operate as x4 modules inside Wide PCIe chassis
- Addresses integrated chassis only, where system module is embedded within a chassis.

AXIe Wide PCIe - Summary

- Each AXIe-1 instrument module currently communicates with the system module using FC1 (Fabric Channel 1) to create a PCIe x4 link.
- Instrument slot FC 2-4 are currently unused.
- Redefine FC 2-4 as optional fabric for wide PCIe:



Wide PCIe assumes an integrated chassis with embedded system module. Example:

2-slot 2U integrated chassis

5-slot 4U integrated chassis

Embedded system modules (ESMs) allow high density routing of Wide PCIe fabric to each instrument slot, avoiding the Slot 1 ASM pin bottleneck.

Integrated chassis are the most prevalent form of AXIe chassis in the market.

Typically, the test system controller is external, connecting to the ESM via a Cable PCIe link. A test system controller may also be installed into one of the instrument slots.

Attainable Throughput (in GByte/s)

Theoretical:

GByte/s	Gen 2	Gen 3
PCIe x1 GBps	0.50	0.98
PCIe x4 GBps	2.00	3.94
PCIe x8 GBps	4.00	7.87
PCIe x16 GBps	8.00	15.74

e.g. 15.74 GByte/s nominal throughout with PCIe Gen 3

Real world:
(80% of
theoretical limit)

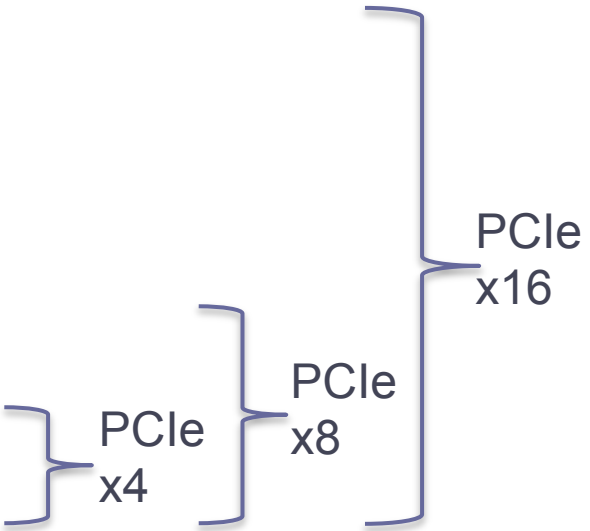
	Gen 2	Gen 3
PCIe x1 GBps	0.40	0.79
PCIe x4 GBps	1.60	3.15
PCIe x8 GBps	3.20	6.30
PCIe x16 GBps	6.40	12.60

AXIe

AXIe Wide PCIe – Instrument slot pin assignments

Row #	Interface Designation	J22/P22 Connector Pairs							
		a b		c d		e f		g h	
1	Fabric Channel 7	Tx2[7]+	Tx2[7]-	Rx2[7]+	Rx2[7]-	Tx3[7]+	Tx3[7]-	Rx3[7]+	Rx3[7]-
2		Tx0[7]+	Tx0[7]-	Rx0[7]+	Rx0[7]-	Tx1[7]+	Tx1[7]-	Rx1[7]+	Rx1[7]-
3	Fabric Channel 6	Tx2[6]+	Tx2[6]-	Rx2[6]+	Rx2[6]-	Tx3[6]+	Tx3[6]-	Rx3[6]+	Rx3[6]-
4		Tx0[6]+	Tx0[6]-	Rx0[6]+	Rx0[6]-	Tx1[6]+	Tx1[6]-	Rx1[6]+	Rx1[6]-
5	Fabric Channel 5	Tx2[5]+	Tx2[5]-	Rx2[5]+	Rx2[5]-	Tx3[5]+	Tx3[5]-	Rx3[5]+	Rx3[5]-
6		Tx0[5]+	Tx0[5]-	Rx0[5]+	Rx0[5]-	Tx1[5]+	Tx1[5]-	Rx1[5]+	Rx1[5]-
7	Fabric Channel 4	Tx2[4]+	Tx2[4]-	Rx2[4]+	Rx2[4]-	Tx3[4]+	Tx3[4]-	Rx3[4]+	Rx3[4]-
8		Tx0[4]+	Tx0[4]-	Rx0[4]+	Rx0[4]-	Tx1[4]+	Tx1[4]-	Rx1[4]+	Rx1[4]-
9	Fabric Channel 3	Tx2[3]+	Tx2[3]-	Rx2[3]+	Rx2[3]-	Tx3[3]+	Tx3[3]-	Rx3[3]+	Rx3[3]-
10		Tx0[3]+	Tx0[3]-	Rx0[3]+	Rx0[3]-	Tx1[3]+	Tx1[3]-	Rx1[3]+	Rx1[3]-

Row #	Interface Designation	J23/P23 Connector Pairs							
		a b		c d		e f		g h	
1	Fabric Channel 2	Tx2[2]+	Tx2[2]-	Rx2[2]+	Rx2[2]-	Tx3[2]+	Tx3[2]-	Rx3[2]+	Rx3[2]-
2		Tx0[2]+	Tx0[2]-	Rx0[2]+	Rx0[2]-	Tx1[2]+	Tx1[2]-	Rx1[2]+	Rx1[2]-
3	Fabric Channel 1	Tx2[1]+	Tx2[1]-	Rx2[1]+	Rx2[1]-	Tx3[1]+	Tx3[1]-	Rx3[1]+	Rx3[1]-
4		Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-	Rx1[1]+	Rx1[1]-



System Management

- No change to system management or e-keying is needed
  - Requires use of the Link Grouping ID to aggregate multiple fabric channels into single links.
- Modules will support the following lane widths, up to the widest land width supported by the module:
  - x1, x2, x4, x8, x16
- PCIe switch will train to widest path
- Flexibility of Fabric Channels 2, 3, and 4 is being reviewed to decrease the number of system management records. This may result in eliminating x1 and x2 for those channels, and/or eliminating Gen 1 for those channels.

Next Steps

- Interoperability testing
- Formalizing specification within AXIe-1
- Consider non-integrated chassis